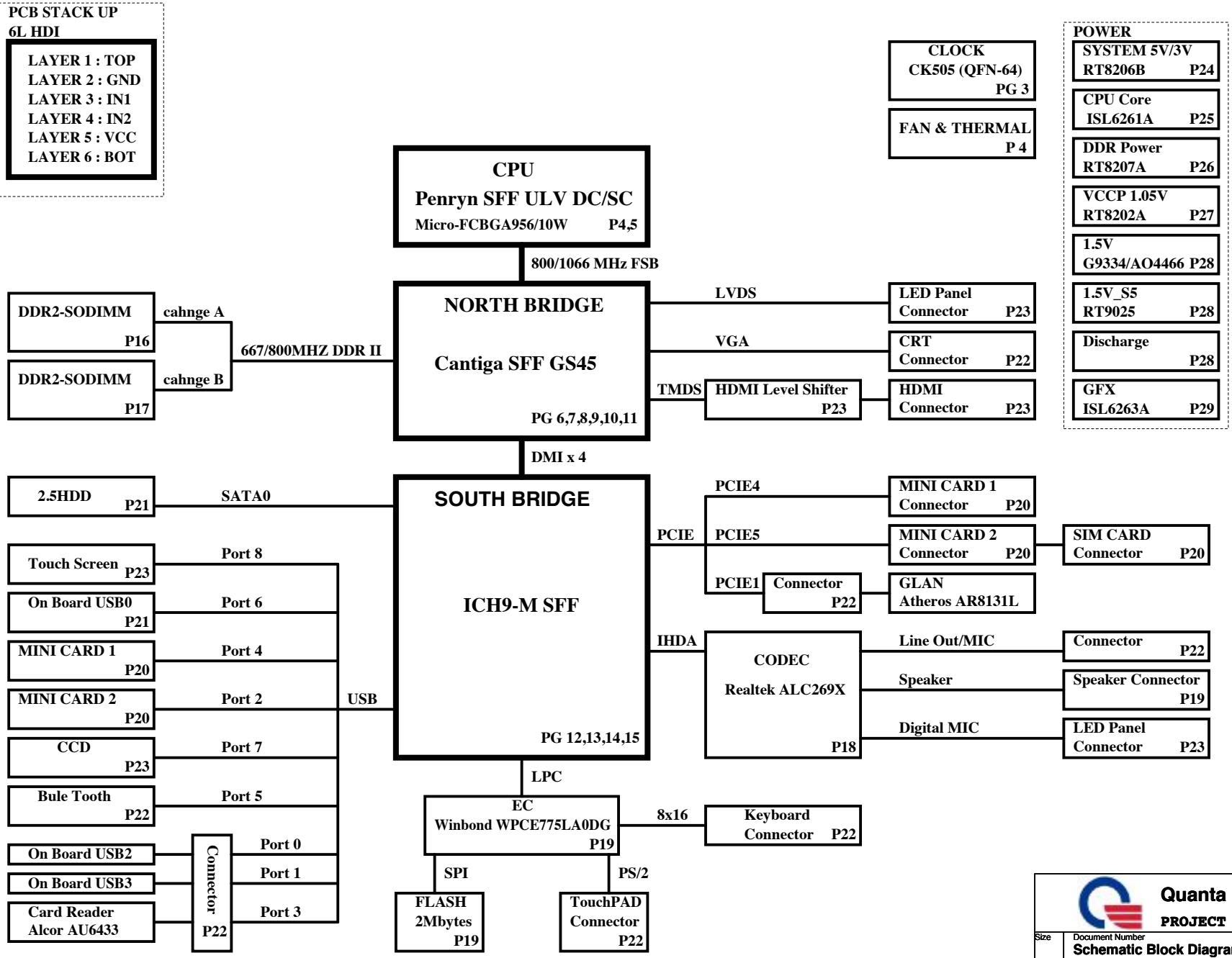
ZE8 BLOCK DIAGRAM



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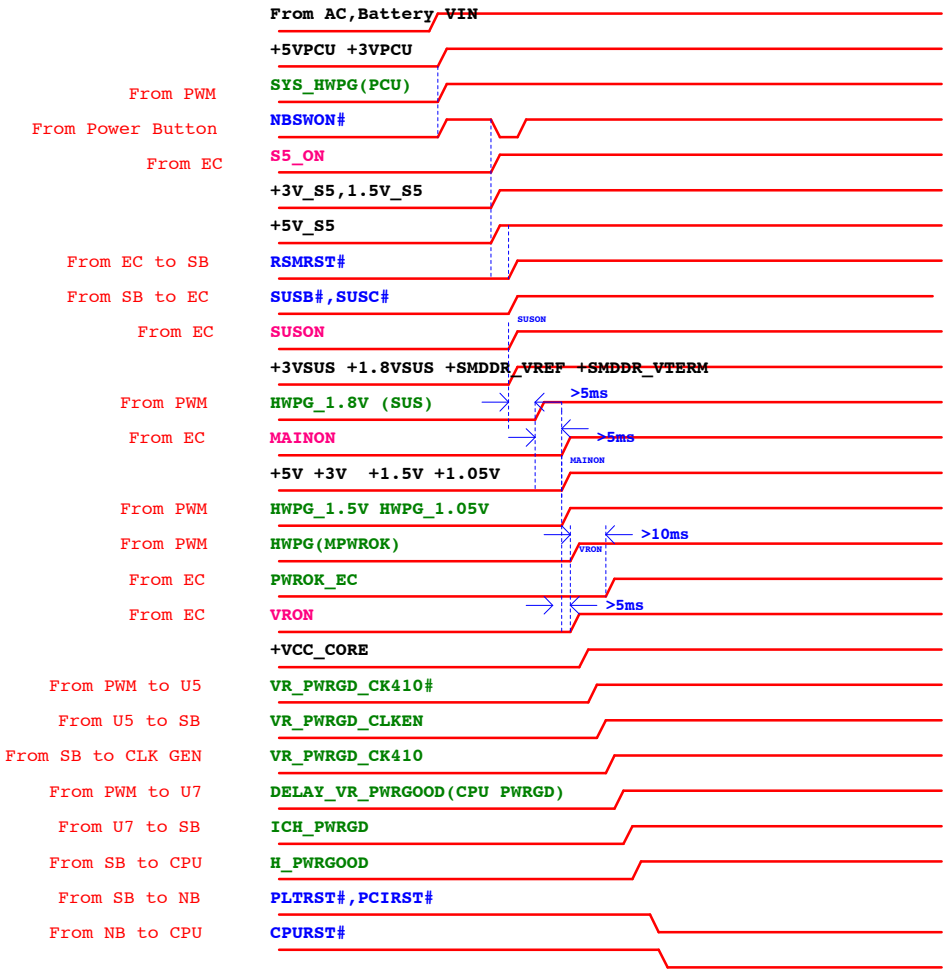
PROJECT : ZE8

Size	Document Number	Rev
	Schematic Block Diagram	1A

Date: Tuesday, September 29, 2009 Sheet 1 of 32

ZE8 Power On Sequence



BOM naming rule

Items	Function	Name	Description
1	With HDMI	HD@	
2	Without HDMI	NHD@	
3	3G Module	3G@	
4			
5			
6			

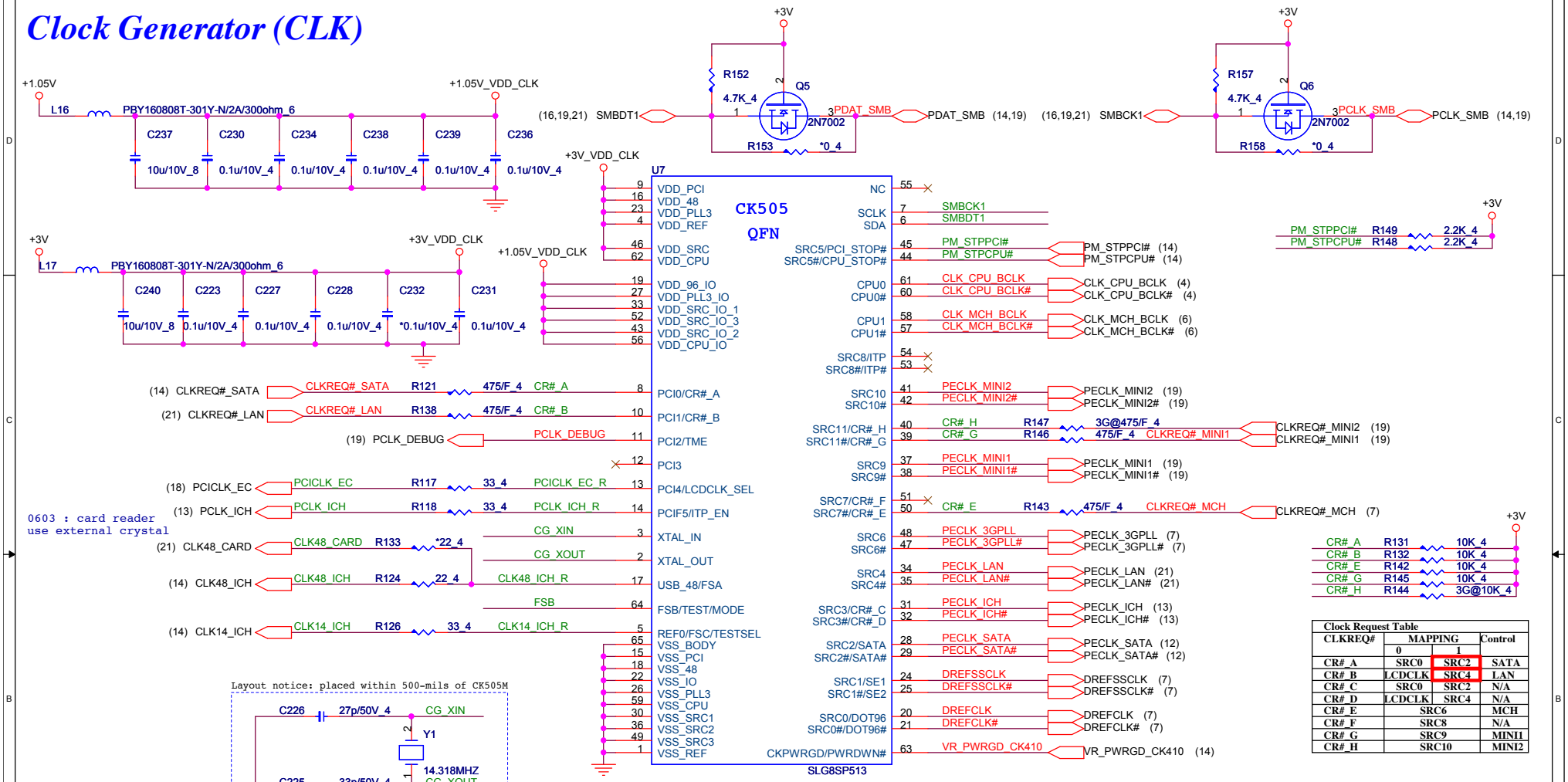
ICH9M SFF SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN/WMAX)	Mini Card (3G)	G sensor
(SMB_DATA) / (SMB_CLK) (+3V_S5)	V	V	V	V	V
Power Plane	+3V	+3V	+3V	+3VSUS	+3V
MOS CKT	Stuff	Stuff	Stuff	Stuff	Stuff

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3V)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X

Clock Generator (CLK)



Clock Request Table			
CLKREQ#	MAPPING 0	MAPPING 1	Control
CR# A	SRC0	SRC2	SATA
CR# B	LCDCLK	SRC4	LAN
CR# C	SRC0	SRC2	N/A
CR# D	LCDCLK	SRC4	N/A
CR# E	SRC6		MCH
CR# F	SRC8		N/A
CR# G	SRC9		MINI1
CR# H	SRC10		MINI2

	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ 27_Select	PCI_4/ SEL_LCDCLK#	PIN 24/25 IS 27MHz	PIN 24/25 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

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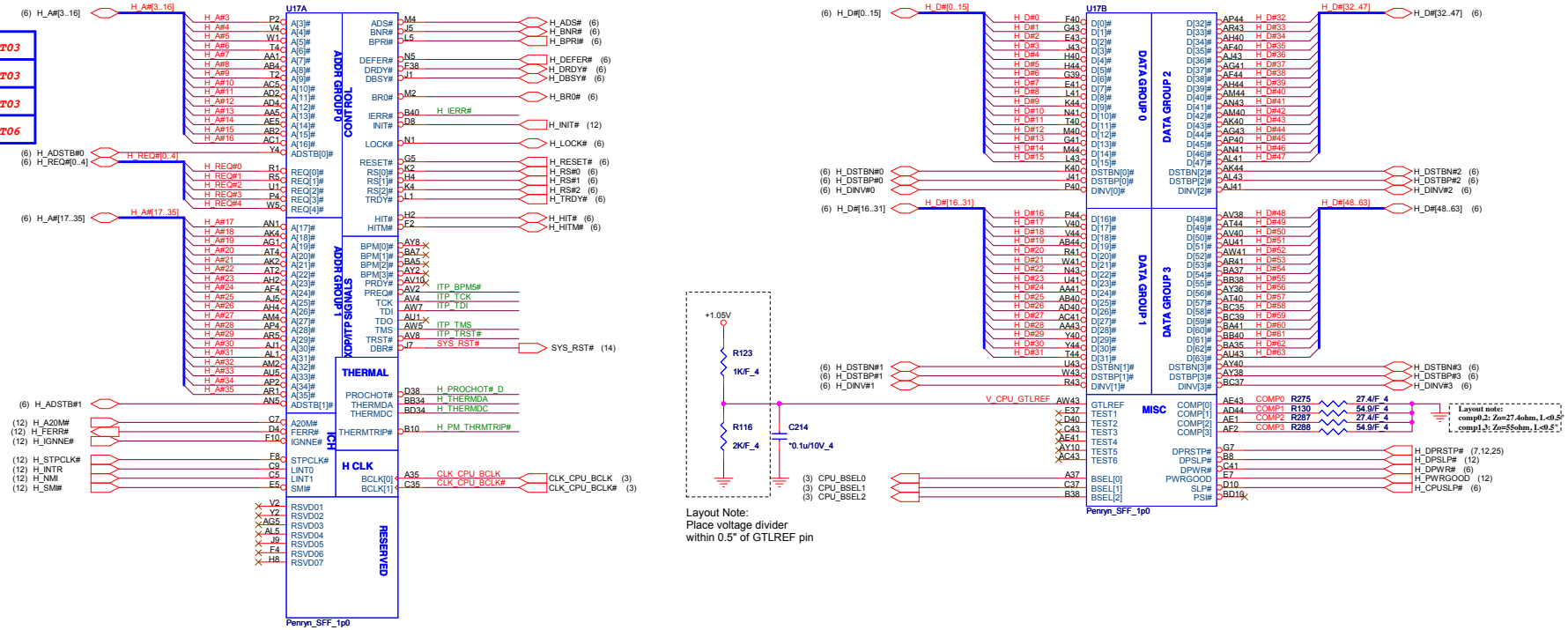
PROJECT : ZE8

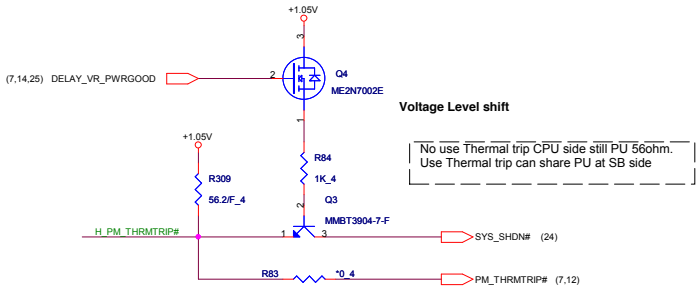
Size	Document Number	Rev
	CLOCK GENERATOR CK505	1A

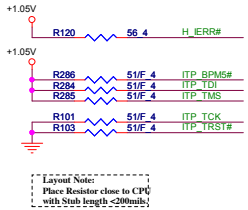
Date: Tuesday, September 29, 2009 Sheet 3 of 32

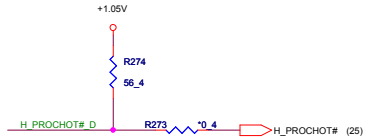
Penryn SFF - Host Bus (CPU)

Celeron 743	AJSLGEVVT03
SU2300	AJSLGYWVT03
SU4100	AJSLGS4VT03
SU7300	AJSLGYVVT06

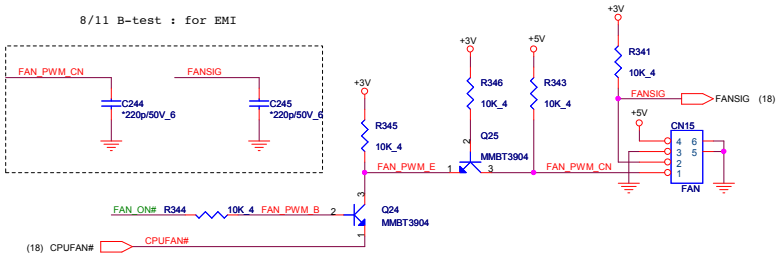




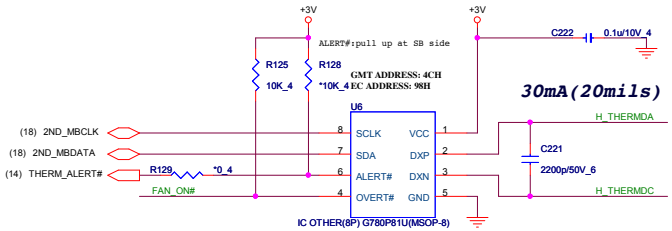




CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



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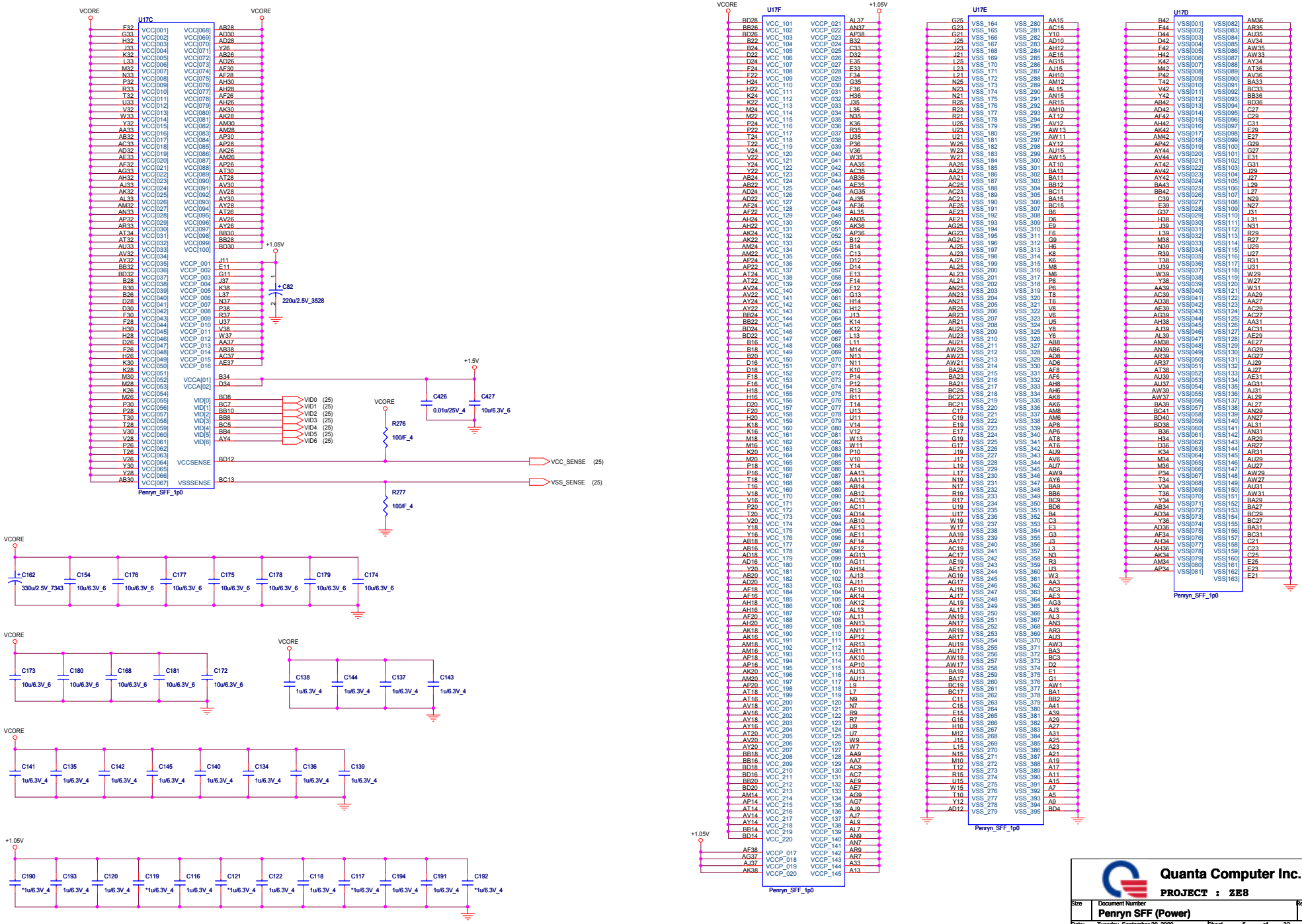
PROJECT : ZE8

Size	Document Number	Rev
	Penryn SFF (Host Bus)/FAN/Thermal	1A

Date: Tuesday, September 29, 2009 Sheet 4 of 32

Penryn SFF - Power (CPU)



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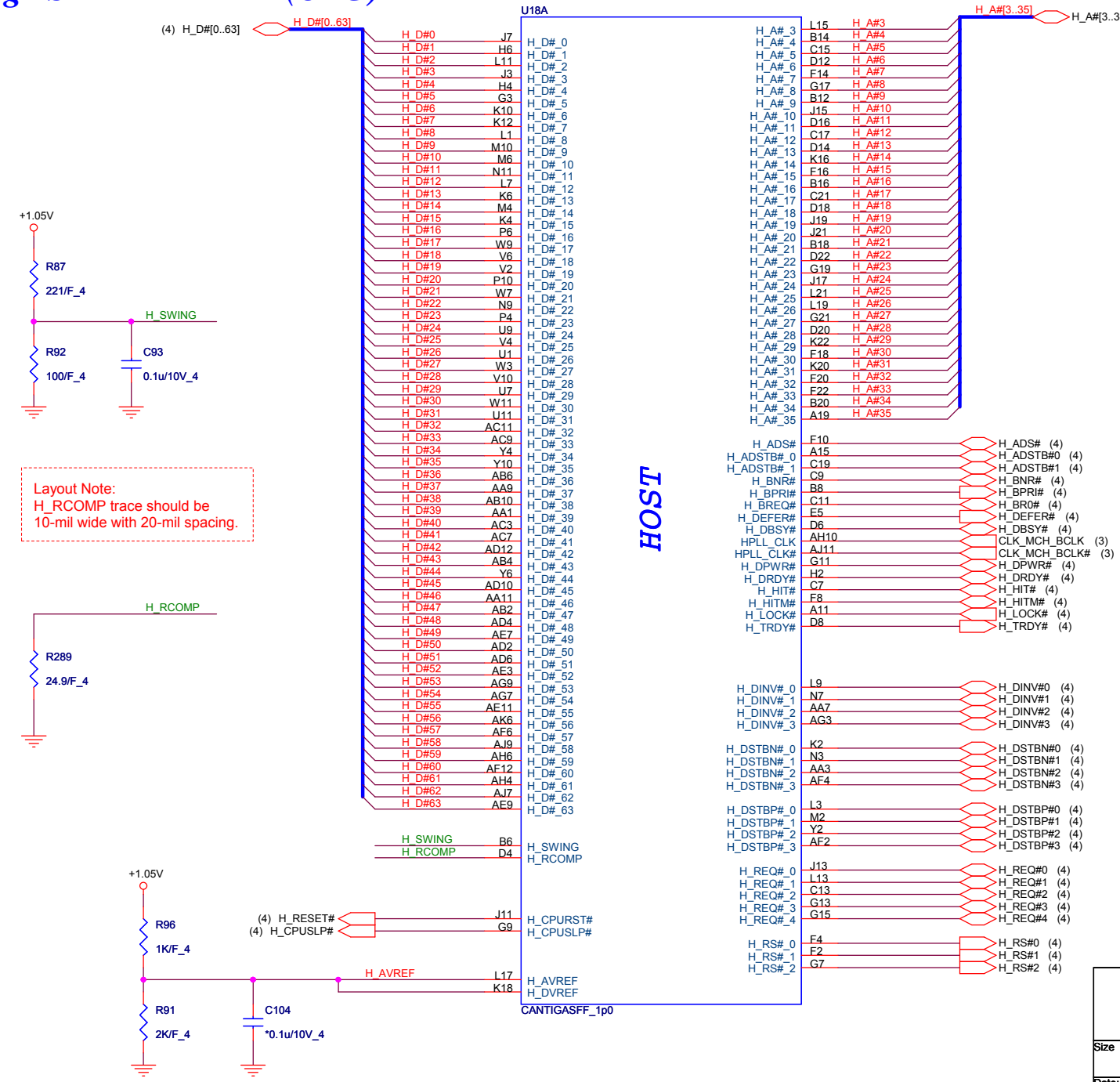
PROJECT : ZE8

Size	Document Number	Rev
	Penryn SFF (Power)	1A

Date: Tuesday, September 29, 2009 Sheet 5 of 32

Cantiga SFF - Host Bus (CLG)



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PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (Host Bus)	1A

Date: Tuesday, September 29, 2009 Sheet 6 of 32

Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation ; Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation ; Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/iHDMI/DP interface enabled 0 = No SDVO/iHDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) device present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 k Ω ±1%
- The recommended pull-down resistor value is 2.21 k Ω ±1%.

U18B

RSVD: RSVD1 (J43), RSVD2 (L43), RSVD3 (J41), RSVD4 (L41), RSVD5 (AN11), RSVD6 (AM10), RSVD7 (AK10), RSVD8 (AL11), RSVD9 (F12), RSVD14 (C27), RSVD15 (D30), RSVD17 (J9), RSVD20 (AW42), RSVD22 (BB20), RSVD23 (BE19), RSVD24 (BF20), RSVD25 (BF18)

ME_JTAG_TCK (AN45), ME_JTAG_TDI (AP44), ME_JTAG_TDO (AT44), ME_JTAG_TMS (AN47)

DDR CLK/ CONTROL/COMPENSATION

SA_CK_0	BB32	M_CLK_DDR0	(16)
SA_CK_1	BA25	M_CLK_DDR1	(16)
SB_CK_0	BA33	M_CLK_DDR2	(16)
SB_CK_1	BA23	M_CLK_DDR3	(16)
SA_CK#_0	BA31	M_CLK_DDR#0	(16)
SA_CK#_1	BC25	M_CLK_DDR#1	(16)
SB_CK#_0	BC33	M_CLK_DDR#2	(16)
SB_CK#_1	BB24	M_CLK_DDR#3	(16)
SA_CKE_0	BC35	M_CKE0	(16)
SA_CKE_1	BB33	M_CKE1	(16)
SB_CKE_0	BE37	M_CKE2	(16)
SB_CKE_1	BC37	M_CKE3	(16)
SA_CS#_0	BK18	M_CS#0	(16)
SA_CS#_1	BK16	M_CS#1	(16)
SB_CS#_0	BE23	M_CS#2	(16)
SB_CS#_1	BC19	M_CS#3	(16)
SA_ODT_0	BJ17	M_ODT0	(16)
SA_ODT_1	BJ19	M_ODT1	(16)
SB_ODT_0	BC17	M_ODT2	(16)
SB_ODT_1	BE17	M_ODT3	(16)
SM_RCOMP	BL25	SMRCOMPP	
SM_RCOMP#	BK26	SMRCOMPN	
SM_RCOMP_VOH	BK32	SM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	SM_RCOMP_VOL	
SM_VREF	BC51	+SMDDR_VREF_NB	
SM_PWROK	AY37	SM_PWROK	
SM_REXT	BH20	SM_REXT	
SM_DRAMRST#	BA37	DDR3_RST#	(16)

SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

CLK

DPLL_REF_CLK	B42	DREFCLK#	DREFCLK (3)
DPLL_REF_CLK#	D42	DREFCLK#	DREFCLK# (3)
DPLL_REF_SSCLK	B50	DREFSSCLK	DREFSSCLK (3)
DPLL_REF_SSCLK#	D50	DREFSSCLK#	DREFSSCLK# (3)
PEG_CLK	R49	PECLK_3GPLL	PECLK_3GPLL (3)
PEG_CLK#	P50	PECLK_3GPLL#	PECLK_3GPLL# (3)

DMI

DMI_RXN_0	AG55	DMI_MRX_ITX_N0	(13)
DMI_RXN_1	AL49	DMI_MRX_ITX_N1	(13)
DMI_RXN_2	AH54	DMI_MRX_ITX_N2	(13)
DMI_RXN_3	AL47	DMI_MRX_ITX_N3	(13)
DMI_RXP_0	AG53	DMI_MRX_ITX_P0	(13)
DMI_RXP_1	AK50	DMI_MRX_ITX_P1	(13)
DMI_RXP_2	AH52	DMI_MRX_ITX_P2	(13)
DMI_RXP_3	AL45	DMI_MRX_ITX_P3	(13)
DMI_TXN_0	AG49	DMI_MTX_IRX_N0	(13)
DMI_TXN_1	AJ49	DMI_MTX_IRX_N1	(13)
DMI_TXN_2	AJ47	DMI_MTX_IRX_N2	(13)
DMI_TXN_3	AG47	DMI_MTX_IRX_N3	(13)
DMI_TXP_0	AF50	DMI_MTX_IRX_P0	(13)
DMI_TXP_1	AH50	DMI_MTX_IRX_P1	(13)
DMI_TXP_2	AJ45	DMI_MTX_IRX_P2	(13)
DMI_TXP_3	AG45	DMI_MTX_IRX_P3	(13)

CFG

(3) MCH_BSEL0 — K26 CFG_0
(3) MCH_BSEL1 — G23 CFG_1
(3) MCH_BSEL2 — G25 CFG_2
J25 CFG_3
L25 CFG_4
L27 CFG_5
T10 — MCH_CFG5
F24 CFG_6
T17 — MCH_CFG7
D24 CFG_7
D26 CFG_8
J23 CFG_9
B26 CFG_10
A23 CFG_11
T16 — MCH_CFG12
T15 — MCH_CFG13
C23 CFG_12
B24 CFG_13
B22 CFG_14
K24 CFG_15
T14 — MCH_CFG16
C25 CFG_16
L23 CFG_17
L33 CFG_18
T8 — MCH_CFG19
T9 — MCH_CFG20
K32 CFG_19
K34 CFG_20

PM

(14) PM_SYNC# — J35 PM_SYNC#
(4,12,25) H_DPRSTP# — F6 PM_DPRSTP#
(16) PM_EXTTS#0 — PM_EXTTS#0 — J39 PM_EXT_TS#_0
(16) PM_EXTTS#1 — PM_EXTTS#1 — L39 PM_EXT_TS#_1
(4,14,25) DELAY_VR_PWRGOOD — AY39 PWROK
(13,18,19,21) PLTRST# — R136 100_4 — RSTIN#_MCH — BB18 RSTIN#
(4,12) PM_THRMTRIP# — R98 0_4 — K28 THERMTRIP#
(14,25) DPRSLPVR — K36 DPRSLPVR

GRAPHICS VID

GFX_VID_0	G33	GPU_VID0	(29)
GFX_VID_1	G37	GPU_VID1	(29)
GFX_VID_2	F38	GPU_VID2	(29)
GFX_VID_3	F36	GPU_VID3	(29)
GFX_VID_4	G35	GPU_VID4	(29)
GFX_VR_EN	G39	GFX_VR_EN	(29)

ME

CL_CLK	AK52	CL_CLK0	(14)
CL_DATA	AK54	CL_DATA0	(14)
CL_PWROK	AW40	MPWROK	(14,18)
CL_RST#	AL53	ICH_CL_RST0#	(14)
CL_VREF	AL55	MCH_CLVREF	

NC

A7 NC_1
A49 NC_2
A52 NC_3
A54 NC_4
B54 NC_5
D55 NC_6
G55 NC_7
BE55 NC_8
BH55 NC_9
BK55 NC_10
BK54 NC_11
BL54 NC_12
BL52 NC_13
BL49 NC_14
BL7 NC_15
BL4 NC_16
BL2 NC_17
BK2 NC_18
BK1 NC_19
BH1 NC_20
BE1 NC_21
G1 NC_22

MISC

DDPC_CTRLCLK	F34	DDPC_CTRLCLK	
DDPC_CTRLDATA	F32	DDPC_CTRLDATA	
SDVO_CTRLCLK	B38	SDVO_CTRLCLK	
SDVO_CTRLDATA	A37	SDVO_CTRLDATA	SDVO_CTRLCLK (22)
CLKREQ#	C31	CLKREQ#_MCH	SDVO_CTRLDATA (22)
ICH_SYNC#	K42	MCH_ICH_SYNC#	CLKREQ#_MCH (3)
			MCH_ICH_SYNC# (14)
TSATN#	D10	TSATN#	

HDA

HDA_BCLK	C29	HDA_BIT_CLK_HDMI	HDA_BIT_CLK_HDMI (12)
HDA_RST#	B30	HDA_RST#_HDMI	HDA_RST#_HDMI (12)
HDA_SDI	D28	HDA_SDIN_HDMI	HDA_SDIN_HDMI (12)
HDA_SDO	A27	HDA_SDOUT_HDMI	HDA_SDOUT_HDMI (12)
HDA_SYNC	B28	HDA_SYNC_HDMI	HDA_SYNC_HDMI (12)

CANTIGASFF_1p0

U18C

PEG_COMPI U45 — PEG_COMPI — R104 49.9/F_4 — +1.05V
PEG_COMPO T44

PEG_RX#_0 D52, PEG_RX#_1 G49, PEG_RX#_2 K54, PEG_RX#_3 H50, PEG_RX#_4 M52, PEG_RX#_5 N49, PEG_RX#_6 P54, PEG_RX#_7 V46, PEG_RX#_8 Y50, PEG_RX#_9 V52, PEG_RX#_10 W49, PEG_RX#_11 AB54, PEG_RX#_12 AD46, PEG_RX#_13 AC55, PEG_RX#_14 AE49, PEG_RX#_15 AF54

PEG_RX_0 E51, PEG_RX_1 F48, PEG_RX_2 J55, PEG_RX_3 J49, PEG_RX_4 M54, PEG_RX_5 M50, PEG_RX_6 P52, PEG_RX_7 U47, PEG_RX_8 AA49, PEG_RX_9 V54, PEG_RX_10 V50, PEG_RX_11 AB52, PEG_RX_12 AC47, PEG_RX_13 AC53, PEG_RX_14 AD50, PEG_RX_15 AF52

PEG_TX#_0 L47, PEG_TX#_1 F52, PEG_TX#_2 P46, PEG_TX#_3 H54, PEG_TX#_4 L55, PEG_TX#_5 T46, PEG_TX#_6 R53, PEG_TX#_7 U49, PEG_TX#_8 T54, PEG_TX#_9 Y46, PEG_TX#_10 AB46, PEG_TX#_11 W55, PEG_TX#_12 Y54, PEG_TX#_13 AC49, PEG_TX#_14 AF46, PEG_TX#_15 AD54

PEG_TX_0 J47, PEG_TX_1 F54, PEG_TX_2 N47, PEG_TX_3 H52, PEG_TX_4 L53, PEG_TX_5 R47, PEG_TX_6 R55, PEG_TX_7 T50, PEG_TX_8 T52, PEG_TX_9 W47, PEG_TX_10 AA47, PEG_TX_11 W55, PEG_TX_12 Y52, PEG_TX_13 AB50, PEG_TX_14 AE47, PEG_TX_15 AD52

PEG_TXN0 C73 — 0.1u/10V_4 — HDMITX2N (22)
PEG_TXN1 C74 — 0.1u/10V_4 — HDMITX1N (22)
PEG_TXN2 C71 — 0.1u/10V_4 — HDMITX0N (22)
PEG_TXN3 C92 — 0.1u/10V_4 — HDMICLKN (22)
PEG_TXP0 C72 — 0.1u/10V_4 — HDMITX2P (22)
PEG_TXP1 C75 — 0.1u/10V_4 — HDMITX1P (22)
PEG_TXP2 C70 — 0.1u/10V_4 — HDMITX0P (22)
PEG_TXP3 C99 — 0.1u/10V_4 — HDMICLKP (22)

HDMI_HP_IV# (22) — HDMI Port B

(22) INT_LVDS_PWM — D38 L_BKLT_CTRL
(22) INT_LVDS_BLON — C37 L_BKLT_EN
L_CTRL_CLK — K38 L_CTRL_CLK
L_CTRL_DATA — L37 L_CTRL_DATA
(22) PHL_CLK — PHL_CLK — J37 L_DDC_DCLK
(22) PHL_DATA — PHL_DATA — L35 L_DDC_DATA
(22) INT_LVDS_DIGON — LVDS_IBG — B36 L_VDD_EN
F50 LVDS_IBG
H46 LVDS_VBG
P44 LVDS_VREFH
K46 LVDS_VREFL
(22) TXLCLKOUT- — TXLCLKOUT- — D46 LVDSA_CLK#
(22) TXLCLKOUT+ — TXLCLKOUT+ — B46 LVDSA_CLK
D44 LVDSB_CLK#
B44 LVDSB_CLK
(22) TXLOUT0- — TXLOUT0- — G45 LVDSA_DATA#_0
(22) TXLOUT1- — TXLOUT1- — F46 LVDSA_DATA#_1
(22) TXLOUT2- — TXLOUT2- — G41 LVDSA_DATA#_2
C45 LVDSA_DATA#_3
(22) TXLOUT0+ — TXLOUT0+ — F44 LVDSA_DATA_0
(22) TXLOUT1+ — TXLOUT1+ — G47 LVDSA_DATA_1
(22) TXLOUT2+ — TXLOUT2+ — F40 LVDSA_DATA_2
A45 LVDSA_DATA_3
B40 LVDSB_DATA#_0
A41 LVDSB_DATA#_1
F42 LVDSB_DATA#_2
D48 LVDSB_DATA#_3
D40 LVDSB_DATA_0
C41 LVDSB_DATA_1
G43 LVDSB_DATA_2
B48 LVDSB_DATA_3

INT_TV_COMP — J27 TVA_DAC
INT_TV_Y/G — E27 TVB_DAC
INT_TV_C/R — G27 TVC_DAC
F26 TVA_RTN
B34 TV_DCONSEL_0
D34 TV_DCONSEL_1

(21) CRT_B — CRT_B — J29 CRT_BLUE
(21) CRT_G — CRT_G — G29 CRT_GREEN
(21) CRT_R — CRT_R — F30 CRT_RED
E29 CRT_IRTN
(21) DDCCLK — D36 CRT_DDC_CLK
(21) DDCDATA — C35 CRT_DDC_DATA
(21) VGAHSYNC — R81 30.1/F_4 — HSYNC — J33 CRT_HSYNC
CRT_IREF — D32 CRT_TVO_IREF
(21) VGAVSYNC — R80 30.1/F_4 — VSYNC — G31 CRT_VSYNC

CANTIGASFF_1p0

PCI-EXPRESS GRAPHICS

VGA

Layout notice: Place the resistor within 500 mils (1.27 mm) of the (G)MCH.

DDR3 PWROK

(18,26,28) SUSON — 1
(18,26) HWPG_+1.5V_SUS — 2
U21 TC7SH08FU — 4 — +3V_S5
At 11/19 change U21 power supply from +3VSUS to +3V_S5
R347 12.1K/F_4 — SM_PWROK
R348 10K_4

CRT setting

R84:
~~if the total motherboard route length is less than 12",~~
the recommended reference resistor value is 1 K Ω ±1%
For longer route lengths between 12" - 15.3" ,
the recommended reference resistor value is 976 Ω ±1%

R93 1.02K/F_4 CRT_IREF

R82 150/F_4 CRT_B
R78 150/F_4 CRT_G
R79 150/F_4 CRT_R

R102 75/F_4 INT_TV_COMP
R291 75/F_4 INT_TV_Y/G
R292 75/F_4 INT_TV_C/R

LVDS setting

+3V
R95 10K_4 L_CTRL_CLK
R94 10K_4 L_CTRL_DATA
R300 2.2K_4 PHL_DATA
R301 2.2K_4 PHL_CLK
R290 2.4K/F_4 LVDS_IBG

Check list note : CL_REF=0.35V

(15mils)

+1.05V — R112 1K/F_4 — MCH_CLVREF — C170 0.1u/10V_4 — R111 511/F_6

DDR3 VREF

(20mils)

+SMDDR_VREF_NB — R113 BLM18BA750SN1D_6 — +SMDDR_VREF
+SMDDR_VREF_NB — R350 *10K/F_4 — R349 *10K/F_4 — +1.5V_SUS

+SMDDR_VREF_NB.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

TSATN# — R296 56_4 — +1.05V
PM_EXTTS#0 — R100 10K_4 — +3V
PM_EXTTS#1 — R97 10K_4
SM_REXT — R271 499/F_4

DDR3 RCOMP

SMRCOMPP — R270 80.6/F_4 — +1.5V_SUS
SMRCOMPN — R272 80.6/F_4

DDR3 RCOMP_VOH/VOL

+1.5V_SUS — R264 1K/F_4 — SM_RCOMP_VOH
R269 3.01K/F_4 — C423 0.01u/25V_4 — C421 2.2u/6.3V_6
SM_RCOMP_VOL
R266 1K/F_4 — C422 0.01u/25V_4 — C418 2.2u/6.3V_6

+3V
DDPC_CTRLCLK R294 2.2K_4
DDPC_CTRLDATA R295 2.2K_4
SDVO_CTRLCLK R297 4.7K_4
SDVO_CTRLDATA R299 4.7K_4
CLKREQ#_MCH R293 10K_4

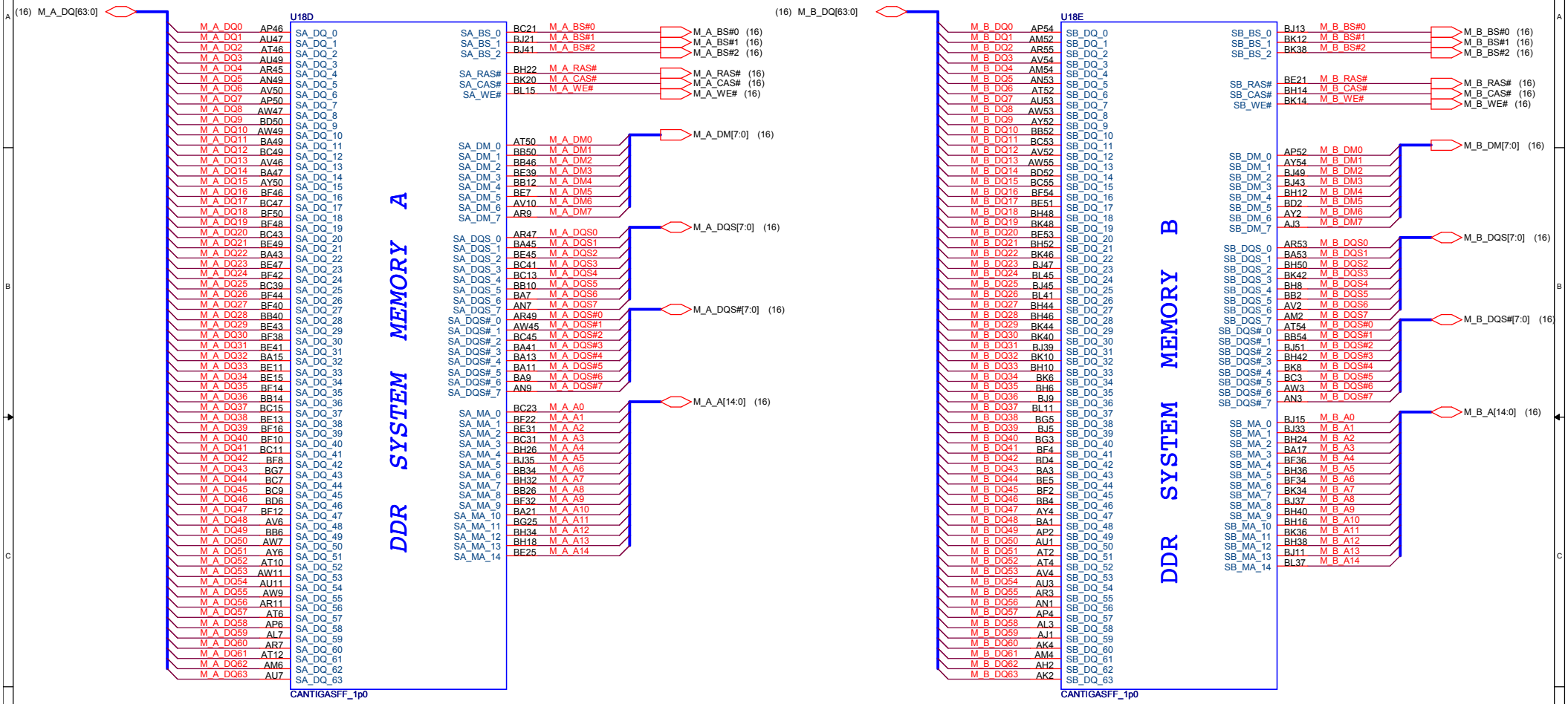
(7/7) intel check list 360543 rev 2.0 CLKREQ# need to 10K pull high to 3.3V

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (DMI/VGA)	1A

Date: Tuesday, September 29, 2009 Sheet 7 of 32

Cantiga SFF - DDRII (CLG)



Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (DDRII)	1A

Date: Tuesday, September 29, 2009 Sheet 8 of 32

Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

VCC 2200mA

U18F

+1.05V

VCC_1, VCC_2, VCC_3, VCC_4, VCC_5, VCC_6, VCC_7, VCC_8, VCC_9, VCC_10, VCC_11, VCC_12, VCC_13, VCC_14, VCC_15, VCC_16, VCC_17, VCC_18, VCC_19, VCC_20, VCC_21, VCC_22, VCC_23, VCC_24, VCC_25, VCC_26, VCC_27, VCC_28, VCC_29, VCC_30, VCC_31, VCC_32, VCC_33, VCC_34, VCC_35, VCC_36, VCC_37, VCC_38, VCC_39, VCC_40, VCC_41, VCC_42, VCC_43, VCC_44, VCC_45, VCC_46, VCC_47, VCC_48, VCC_49, VCC_50, VCC_51, VCC_52, VCC_53, VCC_54, VCC_55, VCC_56, VCC_57, VCC_58, VCC_59, VCC_60, VCC_61

VCC CORE

POWER

VCC NCTF

VCC_NCTF_1, VCC_NCTF_2, VCC_NCTF_3, VCC_NCTF_4, VCC_NCTF_5, VCC_NCTF_6, VCC_NCTF_7, VCC_NCTF_8, VCC_NCTF_9, VCC_NCTF_10, VCC_NCTF_11, VCC_NCTF_12, VCC_NCTF_13, VCC_NCTF_14, VCC_NCTF_15, VCC_NCTF_16, VCC_NCTF_17, VCC_NCTF_18, VCC_NCTF_19, VCC_NCTF_20, VCC_NCTF_21, VCC_NCTF_22, VCC_NCTF_23, VCC_NCTF_24, VCC_NCTF_25, VCC_NCTF_26, VCC_NCTF_27, VCC_NCTF_28, VCC_NCTF_29, VCC_NCTF_30, VCC_NCTF_31, VCC_NCTF_32, VCC_NCTF_33, VCC_NCTF_34, VCC_NCTF_35, VCC_NCTF_36, VCC_NCTF_37, VCC_NCTF_38

CANTIGASFF_1p0

VCC_SM(+1.5V_SUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

+1.5V_SUS

+VCC_SM_BB36, +VCC_SM_BE35

C217 0.1u/10V_4, C216 0.1u/10V_4

VCC_SM :3000mA

+VCC_SM_BC29

C213 0.1u/10V_4

+VCC_SM_BF24, +VCC_SM_BL19, +VCC_SM_BB16

C209 0.1u/10V_4, C424 0.1u/10V_4, C206 0.1u/10V_4

U18G

VCC_SM_1, VCC_SM_2, VCC_SM_3, VCC_SM_4, VCC_SM_5, VCC_SM_6, VCC_SM_7, VCC_SM_8, VCC_SM_9, VCC_SM_10, VCC_SM_11, VCC_SM_12, VCC_SM_13, VCC_SM_14, VCC_SM_15, VCC_SM_16, VCC_SM_17, VCC_SM_18, VCC_SM_19, VCC_SM_20, VCC_SM_21, VCC_SM_22, VCC_SM_23, VCC_SM_24, VCC_SM_25, VCC_SM_26, VCC_SM_27, VCC_SM_28, VCC_SM_29, VCC_SM_30, VCC_SM_31, VCC_SM_32, VCC_SM_33

VCC SM

POWER

VCC GFX NCTF

VCC_AXG_NCTF_1, VCC_AXG_NCTF_2, VCC_AXG_NCTF_3, VCC_AXG_NCTF_4, VCC_AXG_NCTF_5, VCC_AXG_NCTF_6, VCC_AXG_NCTF_7, VCC_AXG_NCTF_8, VCC_AXG_NCTF_9, VCC_AXG_NCTF_10, VCC_AXG_NCTF_11, VCC_AXG_NCTF_12, VCC_AXG_NCTF_13, VCC_AXG_NCTF_14, VCC_AXG_NCTF_15, VCC_AXG_NCTF_16, VCC_AXG_NCTF_17, VCC_AXG_NCTF_18, VCC_AXG_NCTF_19, VCC_AXG_NCTF_20, VCC_AXG_NCTF_21, VCC_AXG_NCTF_22, VCC_AXG_NCTF_23, VCC_AXG_NCTF_24, VCC_AXG_NCTF_25, VCC_AXG_NCTF_26, VCC_AXG_NCTF_27, VCC_AXG_NCTF_28, VCC_AXG_NCTF_29, VCC_AXG_NCTF_30, VCC_AXG_NCTF_31, VCC_AXG_NCTF_32, VCC_AXG_NCTF_33, VCC_AXG_NCTF_34, VCC_AXG_NCTF_35, VCC_AXG_NCTF_36, VCC_AXG_NCTF_37, VCC_AXG_NCTF_38, VCC_AXG_NCTF_39, VCC_AXG_NCTF_40, VCC_AXG_NCTF_41, VCC_AXG_NCTF_42, VCC_AXG_NCTF_43, VCC_AXG_NCTF_44

VCC_AXG_62, VCC_AXG_63, VCC_AXG_64, VCC_AXG_65, VCC_AXG_66, VCC_AXG_67, VCC_AXG_68, VCC_AXG_69, VCC_AXG_70, VCC_AXG_71, VCC_AXG_72, VCC_AXG_73, VCC_AXG_74, VCC_AXG_75, VCC_AXG_76, VCC_AXG_77, VCC_AXG_78, VCC_AXG_79, VCC_AXG_80

VCC GFX

VCC_AXG_1, VCC_AXG_2, VCC_AXG_3, VCC_AXG_4, VCC_AXG_5, VCC_AXG_6, VCC_AXG_7, VCC_AXG_8, VCC_AXG_9, VCC_AXG_10, VCC_AXG_11, VCC_AXG_12, VCC_AXG_13, VCC_AXG_14, VCC_AXG_15, VCC_AXG_16, VCC_AXG_17, VCC_AXG_18, VCC_AXG_19, VCC_AXG_20, VCC_AXG_21, VCC_AXG_22, VCC_AXG_23, VCC_AXG_24, VCC_AXG_25, VCC_AXG_26, VCC_AXG_27, VCC_AXG_28, VCC_AXG_29, VCC_AXG_30, VCC_AXG_31, VCC_AXG_32, VCC_AXG_33, VCC_AXG_34, VCC_AXG_35, VCC_AXG_36, VCC_AXG_37, VCC_AXG_38, VCC_AXG_39, VCC_AXG_40, VCC_AXG_41, VCC_AXG_42, VCC_AXG_43, VCC_AXG_44, VCC_AXG_45, VCC_AXG_46, VCC_AXG_47, VCC_AXG_48, VCC_AXG_49, VCC_AXG_50, VCC_AXG_51, VCC_AXG_52, VCC_AXG_53, VCC_AXG_54, VCC_AXG_55, VCC_AXG_56, VCC_AXG_57, VCC_AXG_58, VCC_AXG_59, VCC_AXG_60, VCC_AXG_61

VCC_AXG_SENSE, VSS_AXG_SENSE

VCC_AXG 7700mA

VCC GFX

VCC SM LF

VCC_SM_LF1, VCC_SM_LF2, VCC_SM_LF3, VCC_SM_LF4, VCC_SM_LF5, VCC_SM_LF6, VCC_SM_LF7

AU45 VCCSM_LF1, BF52 VCCSM_LF2, BB38 VCCSM_LF3, BA19 VCCSM_LF4, BE9 VCCSM_LF5, AU9 VCCSM_LF6, AL9 VCCSM_LF7

10mil

C163 0.1u/10V_4, C205 0.1u/10V_4, C204 0.22u/10V_4, C207 0.22u/10V_4, C218 0.47u/6.3V_4, C210 1u/10V_6, C197 1u/10V_6

+VGFX

R108 10/F_4

R107 10/F_4

Differential routing

(29) GFX_VCCSENSE
(29) GFX_VSSSENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

UMA 9.6A(GM45)
(Plane or shape)

+VGFX, +1.05V

R64 *0_8, R65 *0_8, R183 *0_8

Celeron 723,743 not support graphics render standby mode,
so add R64 , R65, del GFX power (Page 29)
SU type cpu support it, so del R64, R65 and add GFX power (Page 29)

9/28: add R183 for voltage low issue

+1.05V

C203 0.1u/10V_4, C182 0.22u/10V_4, C201 0.22u/10V_4, C156 *10u/6.3V_8, C83 *220u/2.5V_3528

Layout Note:
Inside GMCH cavity.

+1.5V_SUS

C200 0.1u/10V_4, C215 10u/6.3V_8, C211 10u/6.3V_8, C212 *10u/6.3V_8

+VGFX

C133 0.47u/6.3V_4, C127 *1u/16V_6, C128 10u/6.3V_6, C115 10u/6.3V_8, C124 0.1u/10V_4, C132 0.1u/10V_4

+VGFX

C108 *220u/2.5V_3528, C107 220u/2.5V_3528

Close to GMCH

Layout Note:
370 mils from edge.

6/13 : add for EMI

+VGFX

C246 *220p/50V_6, C247 *220p/50V_6

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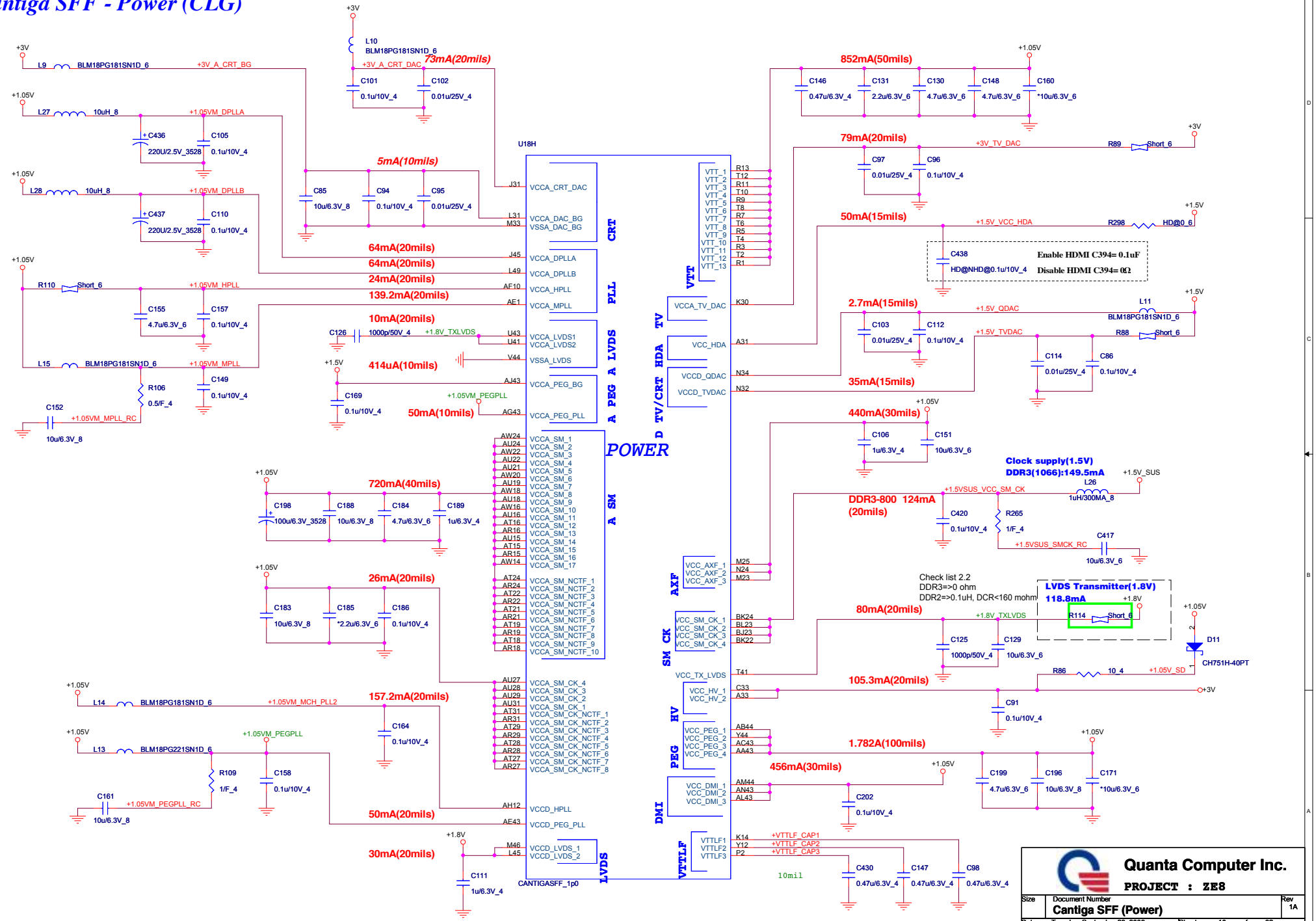
PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (VCC/NCTF)	1A

Date: Tuesday, September 29, 2009 Sheet 9 of 32

Cantiga SFF - Power (CLG)



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PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (Power)	1A

Date: Tuesday, September 29, 2009 Sheet 10 of 32

Cantiga SFF - GND (CLG)

U18I

VSS

BA55	VSS_1	VSS_100	C43
AU55	VSS_2	VSS_101	A43
AN55	VSS_3	VSS_102	BD42
AJ55	VSS_4	VSS_103	H42
AE55	VSS_5	VSS_104	BG41
AA55	VSS_6	VSS_105	AY41
U55	VSS_7	VSS_106	AU41
N55	VSS_8	VSS_107	AM41
BD54	VSS_9	VSS_108	AL41
BG53	VSS_10	VSS_109	AG41
AJ53	VSS_11	VSS_110	AE41
AE53	VSS_12	VSS_111	AA41
AA53	VSS_13	VSS_112	R41
U53	VSS_14	VSS_113	M41
N53	VSS_15	VSS_114	E41
J53	VSS_16	VSS_115	BD40
G53	VSS_17	VSS_116	AU40
E53	VSS_18	VSS_117	AR40
K52	VSS_19	VSS_118	AN40
BG51	VSS_20	VSS_119	W40
BA51	VSS_21	VSS_120	U40
AW51	VSS_22	VSS_121	T40
AU51	VSS_23	VSS_122	R40
AR51	VSS_24	VSS_123	K40
AN51	VSS_25	VSS_124	H40
AL51	VSS_26	VSS_125	BL39
AJ51	VSS_27	VSS_126	BG39
AG51	VSS_28	VSS_127	BA39
AE51	VSS_29	VSS_128	E39
AC51	VSS_30	VSS_129	C39
AA51	VSS_31	VSS_130	A39
W51	VSS_32	VSS_131	BD38
U51	VSS_33	VSS_132	AU38
R51	VSS_34	VSS_133	H38
N51	VSS_35	VSS_134	BG37
L51	VSS_36	VSS_135	AU37
J51	VSS_37	VSS_136	M37
G51	VSS_38	VSS_137	E37
C51	VSS_39	VSS_138	BD36
BK50	VSS_40	VSS_139	AW36
AM50	VSS_41	VSS_140	H36
K50	VSS_42	VSS_141	BL35
BG49	VSS_43	VSS_142	BG35
E49	VSS_44	VSS_143	AY35
C49	VSS_45	VSS_144	AU35
BD48	VSS_46	VSS_145	AL35
BB48	VSS_47	VSS_146	AG35
AY48	VSS_48	VSS_147	AE35
AV48	VSS_49	VSS_148	AA35
AT48	VSS_50	VSS_149	Y35
AP48	VSS_51	VSS_150	M35
AM48	VSS_52	VSS_151	E35
AK48	VSS_53	VSS_152	A35
AH48	VSS_54	VSS_153	BD34
AF48	VSS_55	VSS_154	AU34
AD48	VSS_56	VSS_155	AN34
AB48	VSS_57	VSS_156	H34
Y48	VSS_58	VSS_157	BL33
V48	VSS_59	VSS_158	BG33
T48	VSS_60	VSS_159	AY33
P48	VSS_61	VSS_160	E33
M48	VSS_62	VSS_161	BD32
K48	VSS_63	VSS_162	AU32
H48	VSS_64	VSS_163	AN32
BL47	VSS_65	VSS_164	AG32
BG47	VSS_66	VSS_165	AC32
E47	VSS_67	VSS_166	Y32
C47	VSS_68	VSS_167	H32
A47	VSS_69	VSS_168	B32
BD46	VSS_70	VSS_169	BJ31
AY46	VSS_71	VSS_170	BG31
AM46	VSS_72	VSS_171	AY31
AK46	VSS_73	VSS_172	AN31
AH46	VSS_74	VSS_173	M31
BG45	VSS_75	VSS_174	E31
AE45	VSS_76	VSS_175	N30
AC45	VSS_77	VSS_176	H30
AA45	VSS_78	VSS_177	AN29
W45	VSS_79	VSS_178	AJ29
R45	VSS_80	VSS_179	M29
N45	VSS_81	VSS_180	A29
E45	VSS_82	VSS_181	AW28
BD44	VSS_83	VSS_182	AN28
BB44	VSS_84	VSS_183	AD28
AV44	VSS_85	VSS_184	AC28
AK44	VSS_86	VSS_185	Y28
AH44	VSS_87	VSS_186	W28
AF44	VSS_88	VSS_187	H28
AD44	VSS_89	VSS_188	F28
K44	VSS_90	VSS_189	AN27
H44	VSS_91	VSS_190	AJ27
BL43	VSS_92	VSS_191	M27
BG43	VSS_93	VSS_192	BF26
AY43	VSS_94	VSS_193	BD26
AR43	VSS_95	VSS_194	N26
W43	VSS_96	VSS_195	H26
R43	VSS_97	VSS_196	BJ25
M43	VSS_98	VSS_197	AY25
E43	VSS_99	VSS_198	AU25

CANTIGASFF_1p0

U18J

VSS

AN25	VSS_199	VSS_300	AM8
AG25	VSS_200	VSS_301	AK8
AE25	VSS_201	VSS_302	AH8
AA25	VSS_202	VSS_303	AF8
Y25	VSS_203	VSS_304	AD8
E25	VSS_204	VSS_305	AB8
A25	VSS_205	VSS_306	Y8
BD24	VSS_206	VSS_307	V8
AN24	VSS_207	VSS_308	P8
AL24	VSS_208	VSS_309	M8
H24	VSS_209	VSS_310	K8
BG23	VSS_210	VSS_311	H8
AY23	VSS_211	VSS_312	BJ7
E23	VSS_212	VSS_313	E7
BD22	VSS_213	VSS_314	BF6
BB22	VSS_214	VSS_315	BC5
AN22	VSS_215	VSS_316	BA5
Y22	VSS_216	VSS_317	AW5
W22	VSS_217	VSS_318	AU5
H22	VSS_218	VSS_319	AR5
BL21	VSS_219	VSS_320	AN5
BG21	VSS_220	VSS_321	AL5
AY21	VSS_221	VSS_322	AJ5
AN21	VSS_222	VSS_323	AG5
AG21	VSS_223	VSS_324	AE5
AE21	VSS_224	VSS_325	AC5
M21	VSS_225	VSS_326	AA5
E21	VSS_226	VSS_327	W5
A21	VSS_227	VSS_328	U5
BD20	VSS_228	VSS_329	N5
H20	VSS_229	VSS_330	L5
BG19	VSS_230	VSS_331	J5
AY19	VSS_231	VSS_332	G5
M19	VSS_232	VSS_333	C5
E19	VSS_233	VSS_334	BH4
BD18	VSS_234	VSS_335	BE3
N18	VSS_235	VSS_336	U3
H18	VSS_236	VSS_337	E3
BL17	VSS_237	VSS_338	BC1
BG17	VSS_238	VSS_339	AW1
AY17	VSS_239	VSS_340	AR1
M17	VSS_240	VSS_341	AL1
E17	VSS_241	VSS_342	AG1
A17	VSS_242	VSS_343	AC1
BD16	VSS_243	VSS_344	W1
AN16	VSS_244	VSS_345	N1
AG16	VSS_245	VSS_346	J1
AE16	VSS_246	VSS_347	AU43
Y16	VSS_247	VSS_348	BB42
W16	VSS_248	VSS_349	AW38
N16	VSS_249	VSS_350	BA35
H16	VSS_250	VSS_351	L29
BG15	VSS_251	VSS_352	N28
AY15	VSS_252	VSS_353	N22
AN15	VSS_253	VSS_354	N20
AD15	VSS_254	VSS_355	N14
AC15	VSS_255	VSS_356	AL13
R15	VSS_256	VSS_357	B10
M15	VSS_257	VSS_358	AN13
E15	VSS_258		
BD14	VSS_259	VSS_359	N42
H14	VSS_260	VSS_360	N40
BL13	VSS_261	VSS_361	N38
BG13	VSS_262	VSS_362	M39
AY13	VSS_263		
AU13	VSS_264		
AR13	VSS_265	VSS_NCTF_1	AJ38
AJ13	VSS_266	VSS_NCTF_2	AH38
AC13	VSS_267	VSS_NCTF_3	AD38
AA13	VSS_268	VSS_NCTF_4	AC38
W13	VSS_269	VSS_NCTF_5	T35
U13	VSS_270	VSS_NCTF_6	R35
M13	VSS_271	VSS_NCTF_7	AT32
E13	VSS_272	VSS_NCTF_8	AR32
A13	VSS_273	VSS_NCTF_9	U32
BD12	VSS_274	VSS_NCTF_10	R32
AV12	VSS_275	VSS_NCTF_11	T28
AP12	VSS_276	VSS_NCTF_12	R28
AM12	VSS_277	VSS_NCTF_13	AT25
AK12	VSS_278	VSS_NCTF_14	AR25
AB12	VSS_279	VSS_NCTF_15	T24
V12	VSS_280	VSS_NCTF_16	R24
P12	VSS_281	VSS_NCTF_17	AN19
H12	VSS_282	VSS_NCTF_18	AJ19
BG11	VSS_283	VSS_NCTF_19	AA19
AG11	VSS_284	VSS_NCTF_20	Y19
E11	VSS_285	VSS_NCTF_21	T19
BD10	VSS_286	VSS_NCTF_22	R19
AY10	VSS_287	VSS_NCTF_23	AN18
AP10	VSS_288		
H10	VSS_289		
BL9	VSS_290		
BG9	VSS_291		
E9	VSS_292		
A9	VSS_293	VSS_SCB_1	BL55
BD8	VSS_294	VSS_SCB_2	BL1
BB8	VSS_295	VSS_SCB_3	A55
AY8	VSS_296	VSS_SCB_4	D1
AV8	VSS_297	VSS_SCB_5	B55
AT8	VSS_298	VSS_SCB_6	B2
AP8	VSS_299	VSS_SCB_7	A4

VSS NCTF

VSS SCB

CANTIGASFF_1p0

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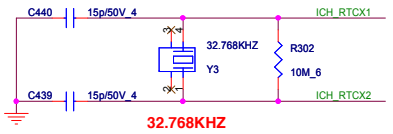
PROJECT : ZE8

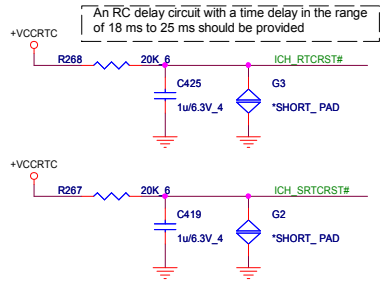
Size	Document Number	Rev
	Cantiga SFF (GND)	1A

Date: Tuesday, September 29, 2009 Sheet 11 of 32

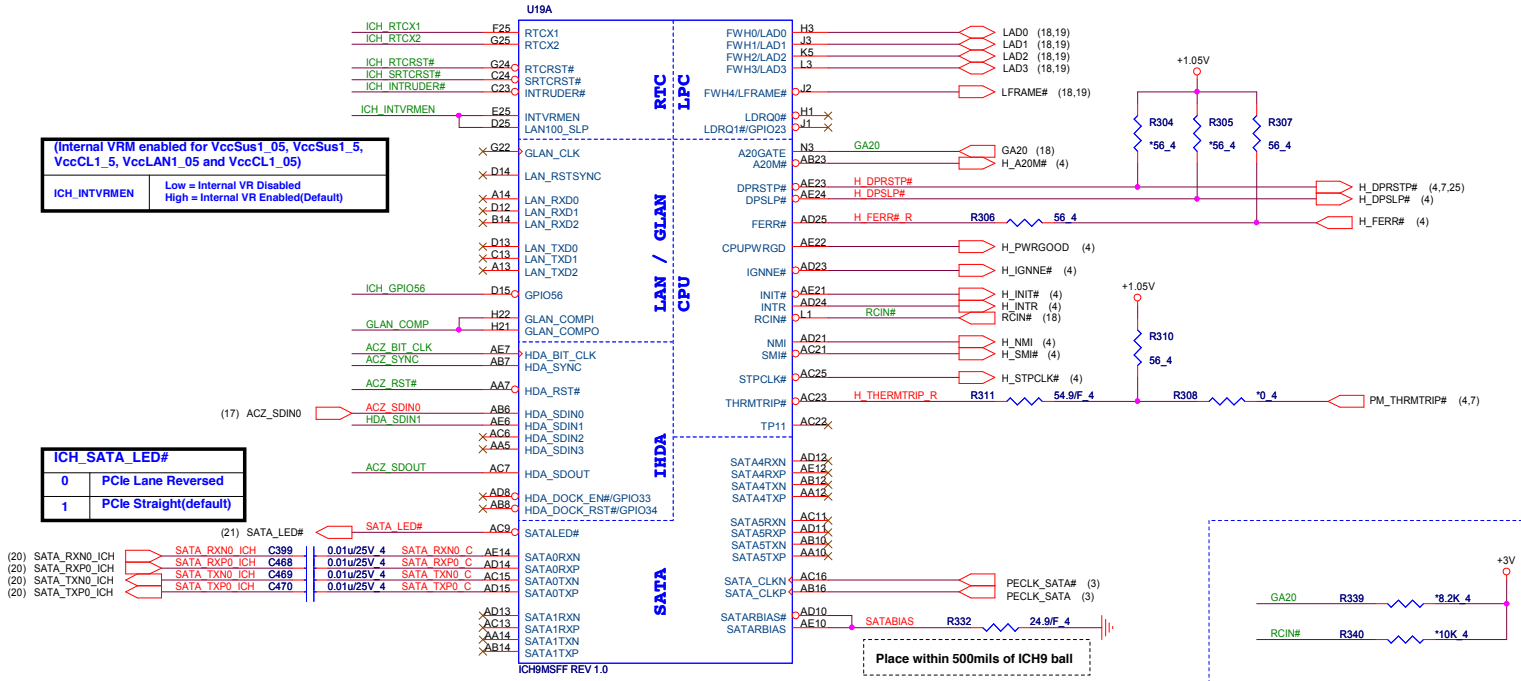
RTC CRYSTAL



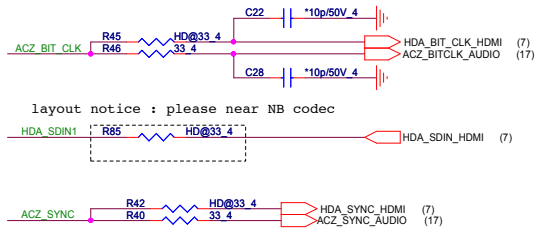
RESET JUMP

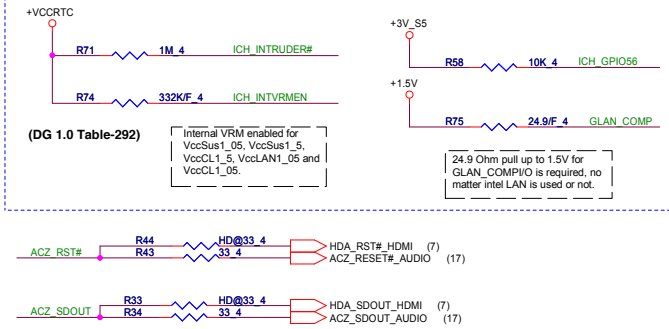


ICH9M SFF - Host,SATA,HDA (CLG)

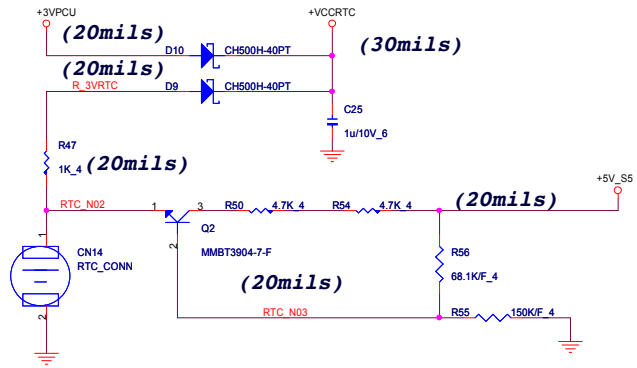


HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD	(14) ICH_TP3 — ICH_TP3 — R316 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	HDA_IO_ICH — R37 — *1K_4 — ACZ_SDOUT R36 — *1K_4 — ACZ_SYNC intel design guide: pull high 3.3k

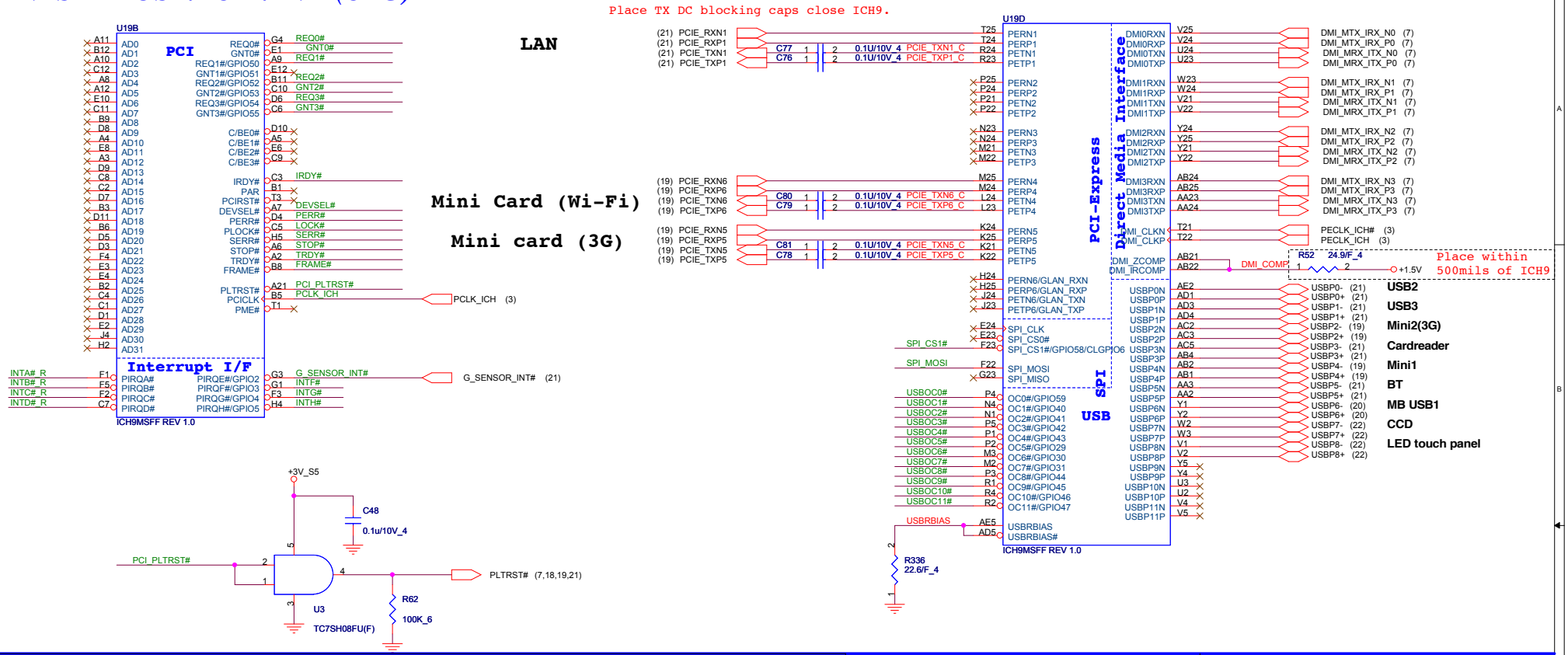
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	ICH9M SFF (Host/SATA/HDA)	1A

Date: Tuesday, September 29, 2009 Sheet 12 of 32

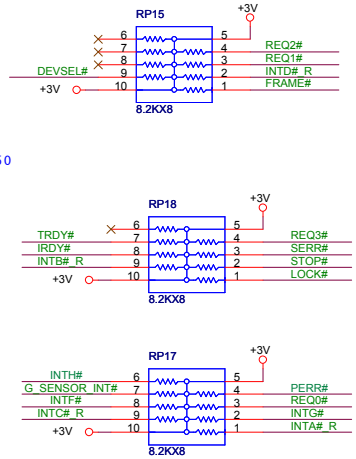
ICH9M SFF - USB/PCIE/DMI (CLG)



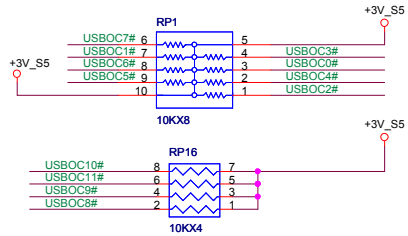
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T20
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	8/28 : add pull high resister R160 in GNT3# pin for no video issue.
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	T3 — GNT3# — R160 10K_4 — +3V
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T18
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default)	GNT0# — T21
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI	SPI_CS1# — T19

PCI PULL-UP



USBOC# PULL-UP



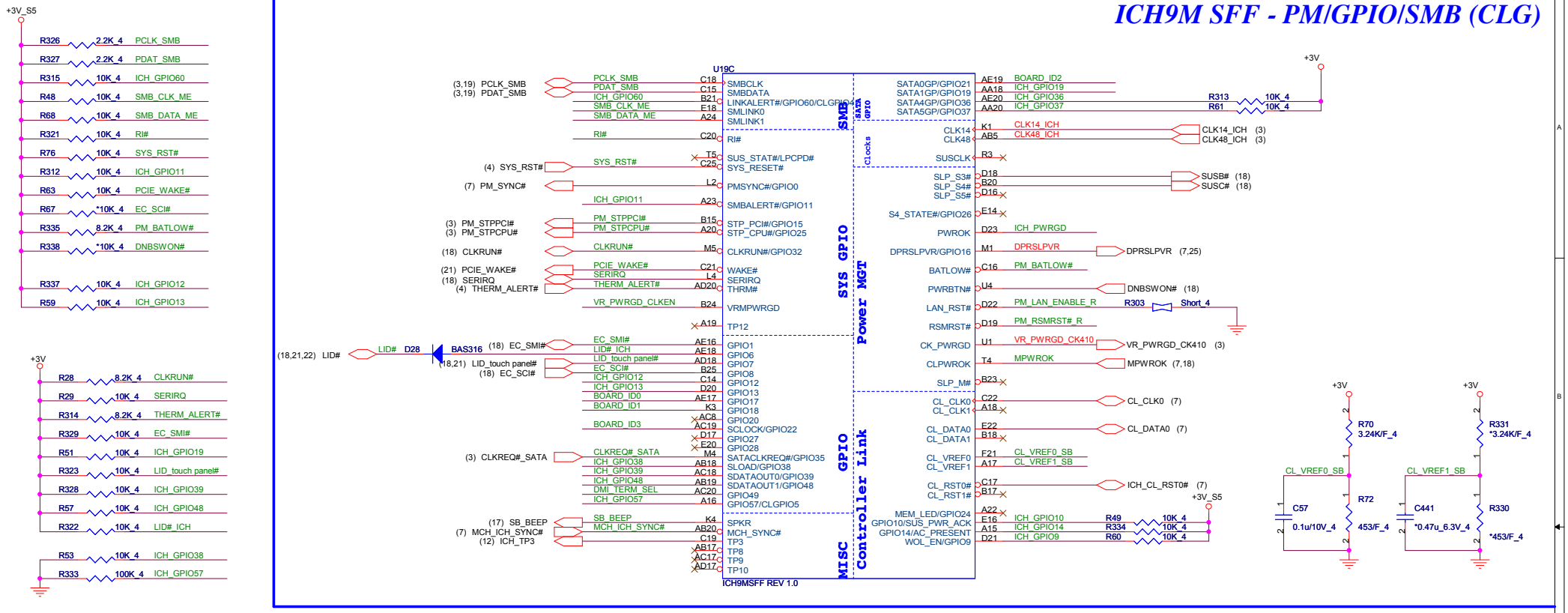
Quanta Computer Inc.

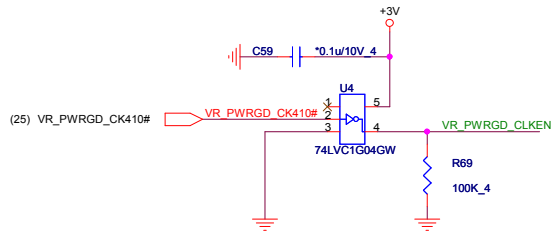
PROJECT : ZE8

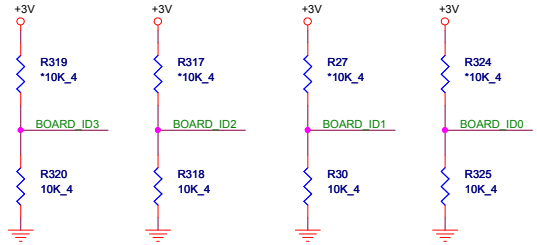
Size	Document Number	Rev
	ICH9M SFF (USB/PCIE/DMI)	1A

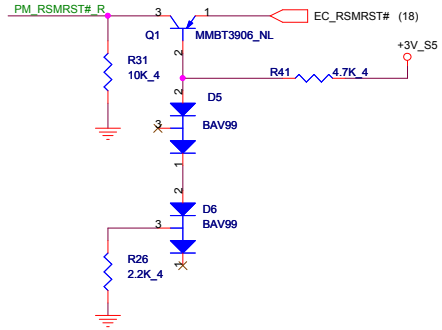
Date: Tuesday, September 29, 2009 Sheet 13 of 32

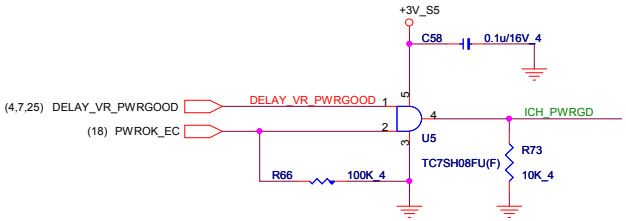
ICH9M SFF - PM/GPIO/SMB (CLG)











South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL — T6

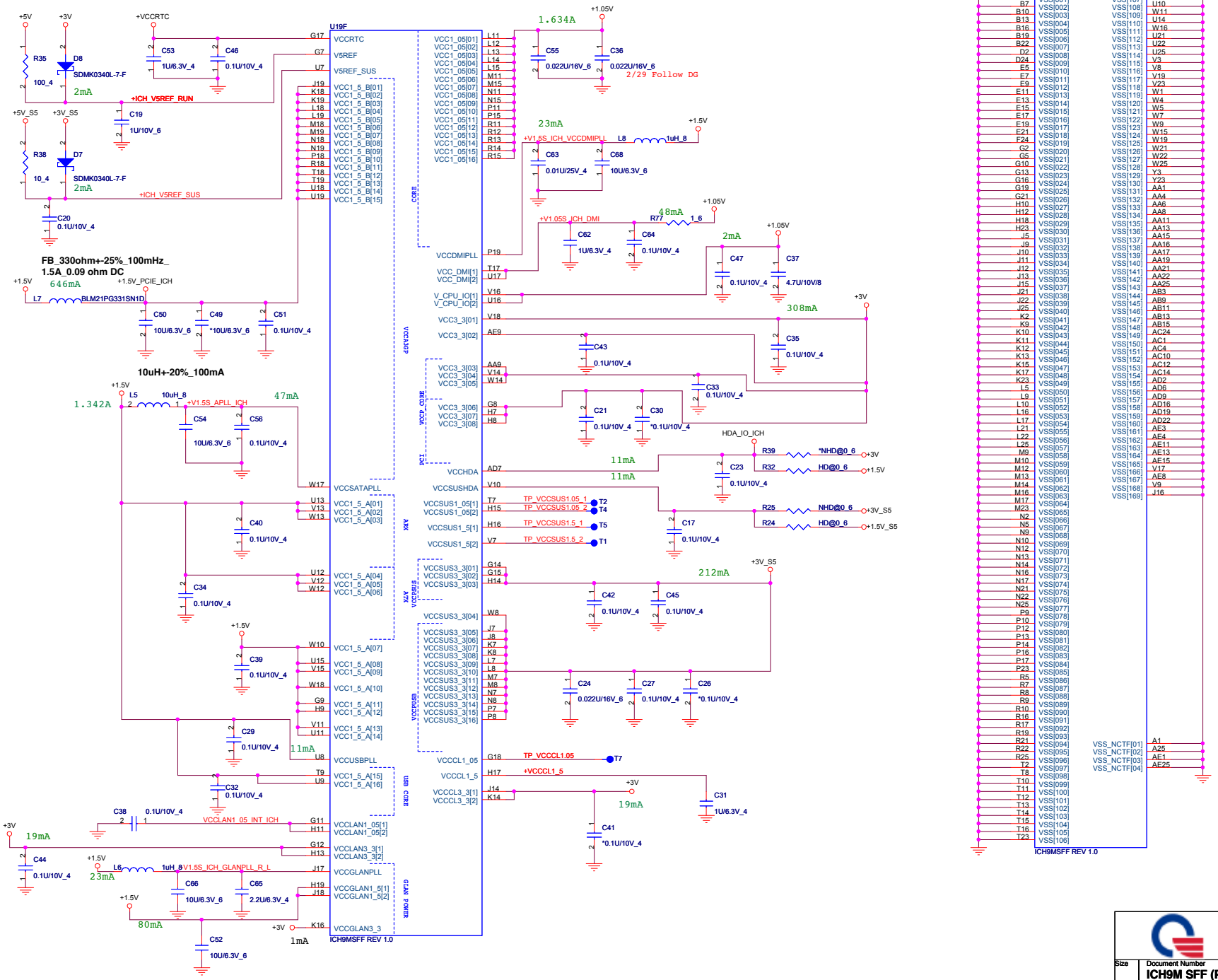
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	ICH9M SFF (PM/GPIO/SMB)	1A

Date: Tuesday, September 29, 2009 Sheet 14 of 32

ICH9M SFF - Power/GND (CLG)

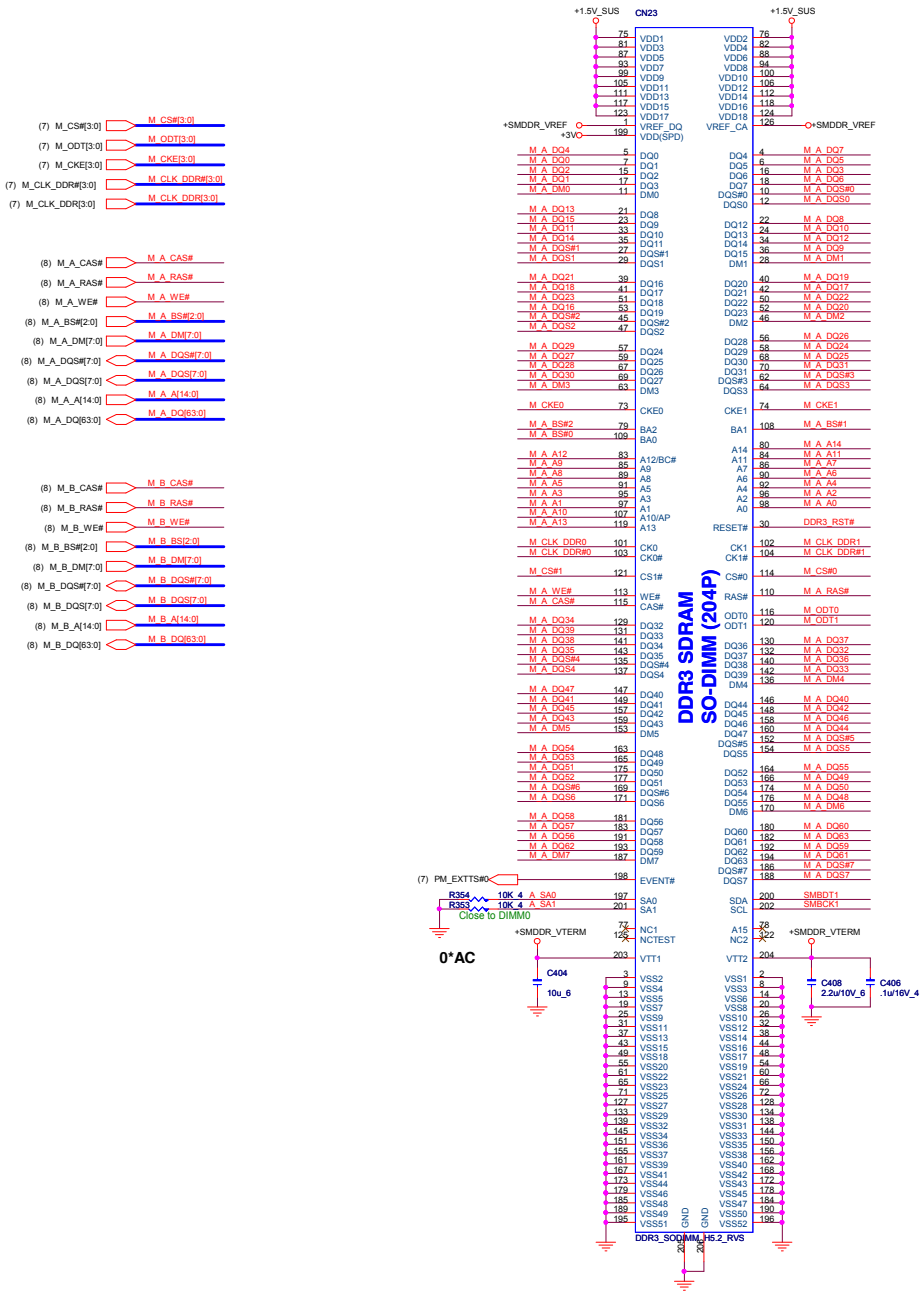


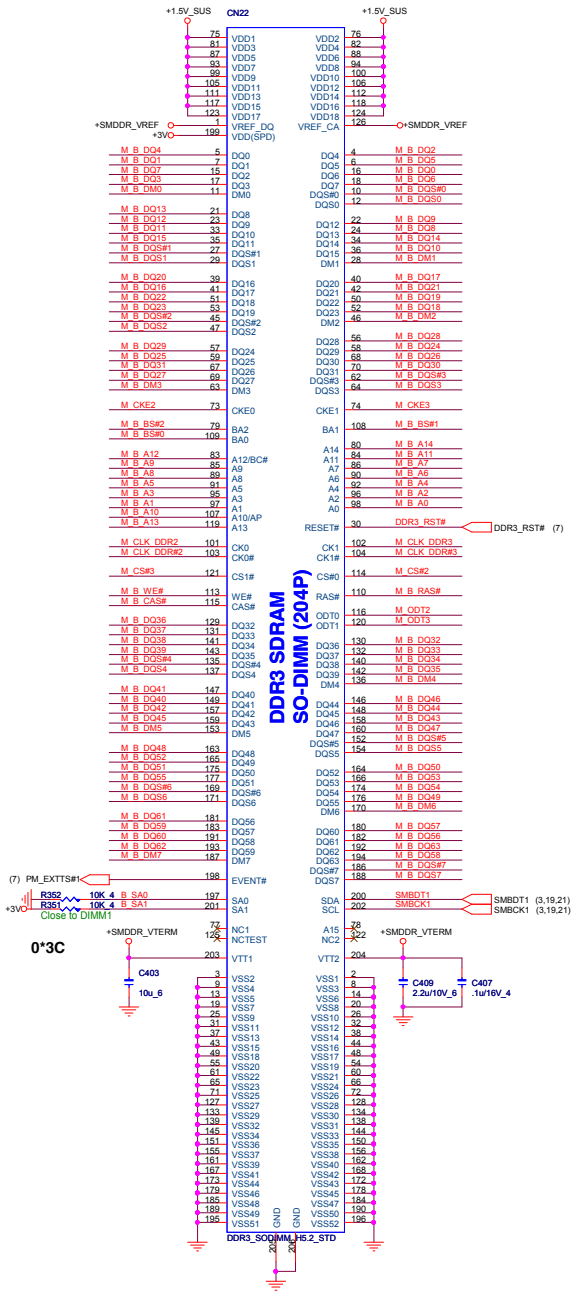
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	ICH9M SFF (Power/GND)	1A

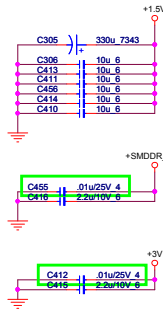
Date: Tuesday, September 29, 2009 Sheet 15 of 32



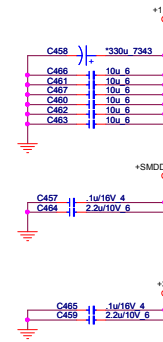


Decoupling capacitor

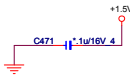
Close to SO-DIMM0



Close to SO-DIMM1



EMI



8/13 : B-test add for EMI

Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	DDRIII SO-DIMM	1A

Date: Tuesday, September 29, 2009 Sheet 16 of 34

Codec ALC269X (ADO)

B-test 8/11: for EMI

SPDIF_OUT
C243 *680p/50V_6
+5VA
C363 0.1U/10V_4

HPOUT-R — HPOUT-R (21)
HPOUT-L — HPOUT-L (21)
MIC1-VREFO-R
MIC1-VREFO-L
Place next to pin 27

ADOGND
C358 2.2U/6.3V_6
C352 2.2U/6.3V_6
C359 *10U/6.3V/6
C353 0.1U/10V/4
C348 0.1U/10V_4
C347 *10U/6.3V_6
Place next to pin 25

U11 ALC269

Spilt by DGND
C350 10U/6.3V_6
C349 0.1U/10V_4
Place next to pin 38

(Vista Premium Version)

Placement near Audio Codec

ANALOG

DIGITAL

1.6Vrms

MIC1_R1
MIC1_L1
R226 20K/F_4
SENSEA
R209 39.2K/F/4 — LINEOUT_JD# (21)
R221 20K/F/4 — MIC1_JD# (21)
(21) SPDIF_OUT — SPDIF_OUT

C342 0.1U/10V_4
C334 10U/6.3V_6
Place next to pin 39

C325 0.1U/10V_4
C327 10U/6.3V_6
Place next to pin 1

C332 0.1U/10V_4
C335 *10U/6.3V_6
Place next to pin 46

(22) DMIC_DAT
(22) DMIC_CLK
PD#

0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer

PCBEEP C324 1u/10V_6 BEEP_1 R198 47K_4 — SB_BEEP (14)
C316 100p/50V_6
R203 2K_4

BOM notice: just can stuff one in BOM
R192 *NHD@0_6 +3V
R189 HD@0_6 +1.5V

+AZA_VDD
C315 0.1U/10V/4
C323 10U/6.3V/_6
Place next to pin 9

ACZ_SDIN
ACZ_RESET#_AUDIO — ACZ_RESET#_AUDIO (12)
ACZ_SYNC_AUDIO (12)
R196 22_4 — ACZ_SDIN0 (12)
C322 10P/50V_4
ACZ_SDOUT_AUDIO (12)
R195 Short_4 — ACZ_BITCLK_AUDIO (12)
C321 *10P/50V_4

Speaker (AMP)

R_SPK+ R242 Short_6 — R_SPK+_1
C357 *0.22U/25V/6
C365 *1u/6.3V_4
C356 *0.22U/25V/6
R_SPK- R241 Short_6 — R_SPK-_1
L_SPK- R240 Short_6 — L_SPK-_1
CN8 Speak CNN
C355 *0.22U/25V/6
C364 *1u/6.3V_4
C354 *0.22U/25V/6
L_SPK+ R239 Short_6 — L_SPK+_1

MIC1-VREFO-R
MIC1-VREFO-L
R238 4.7K/F_4
R237 4.7K/F_4
MIC1_L1 C338 4.7U/6.3V/6 R234 1K/F_4 — MIC1_L2 (21)
MIC1_R1 C341 4.7U/6.3V/6 R233 1K/F_4 — MIC1_R2 (21)

stitching caps for Audio signals
C345 0.1U/10V_4 (+3VPCU — +3V)
C385 0.1U/10V_4 (+3VPCU — +3V)

R259 Short_6
R248 *0_6
R250 *0_6
R243 *0_6
R254 Short_6
C377 *1000p/50V_4
C387 *1000p/50V_4
R247 *0_6
ADOGND

Power (ADO)

R202 *HD@100K_4 — +3V
R188 *HD@100K_4 — +3V
Q15 *HD@2N7002E
Q14 *HD@DTC144EU
ACZ_RESET#_AUDIO
PD#
*NHD@BAS316 D24 ACZ_RESET#_AUDIO
*BAS316 D25 EAPD#
*BAS316 D23 AMP_MUTE# — AMP_MUTE# (18)
R199 Short_4

Demodulation Filter
Place close to Codec

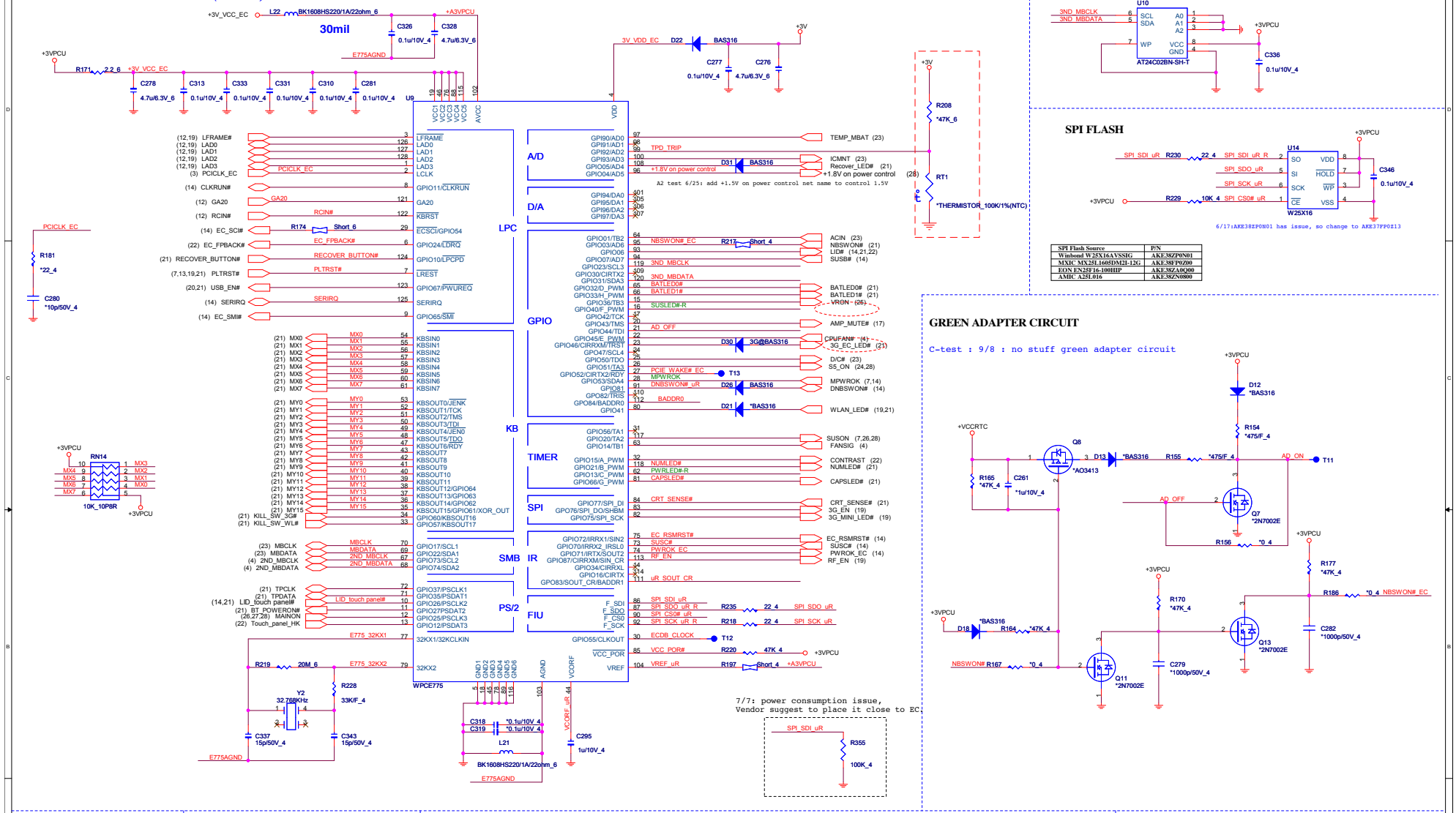
+5V
L25 TI201209U220/8
+5VA
U15 *MAX8863SEUK+T
IN OUT GND SHDN SET
C373 *0.1U/10V/4
R245 *29.4K/F/4
R246 *10K/F/4
C366 *10U/10V/3216
ADOGND

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	Codec ALC269X	1A

Date: Tuesday, September 29, 2009 Sheet 17 of 32

EC WPCE775LA0DG (KBC)



ACER ID

SPI FLASH

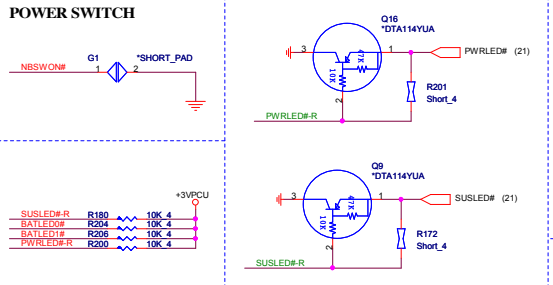
6/17:AKE38ZP0N01 has issue, so change to AKE37FP0Z13

SPI Flash Source	P/N
Winbond W25X16AVSSIG	AKE38ZP0N01
MXIC MX25L1605DM2I-12G	AKE38FP0Z00
EON EN25F16-100HIP	AKE38ZA0Q00
AMIC A25L016	AKE38ZN0B00

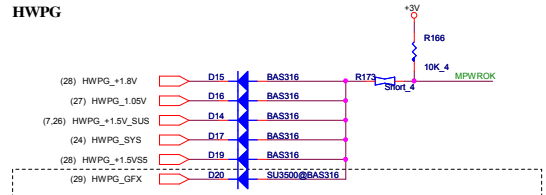
GREEN ADAPTER CIRCUIT

C-test : 9/8 : no stuff green adapter circuit

POWER SWITCH



HWPG



Celeron 723 ,743 not support graphics render standby mode, so del D20
SU7300,SU2300,SU2700,SU4100 support it, so add D20

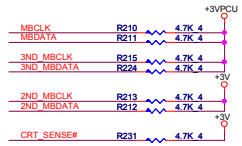
I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 R191 10K_4
BADDR1 — uR_SOUT_CR R193 *10K_4
SHBM — 3G_EN R214 10K_4

SM BUS PU



INTERNAL KEYBOARD STRIP SET

MY0 R187 10K_4 +3VPCU

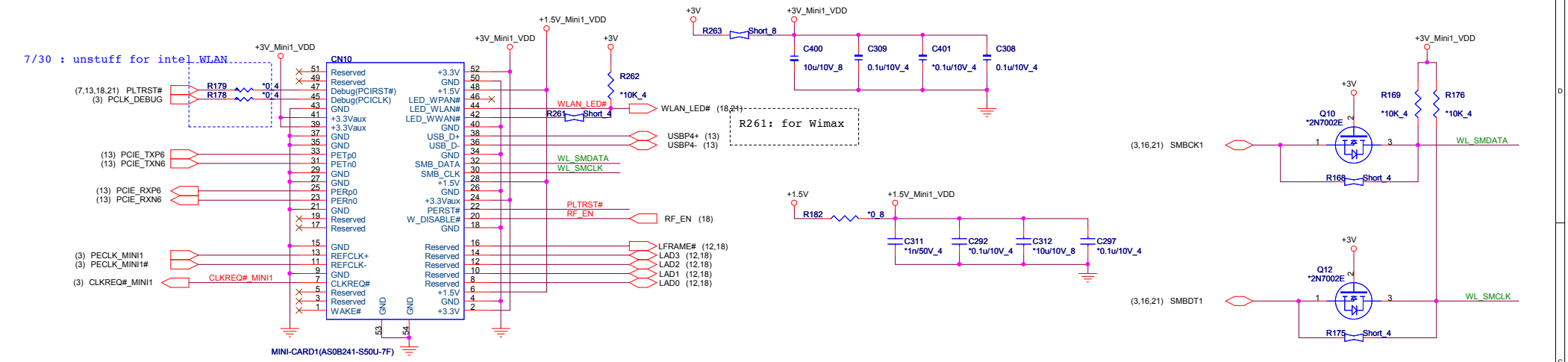
Quanta Computer Inc.

PROJECT : ZE8

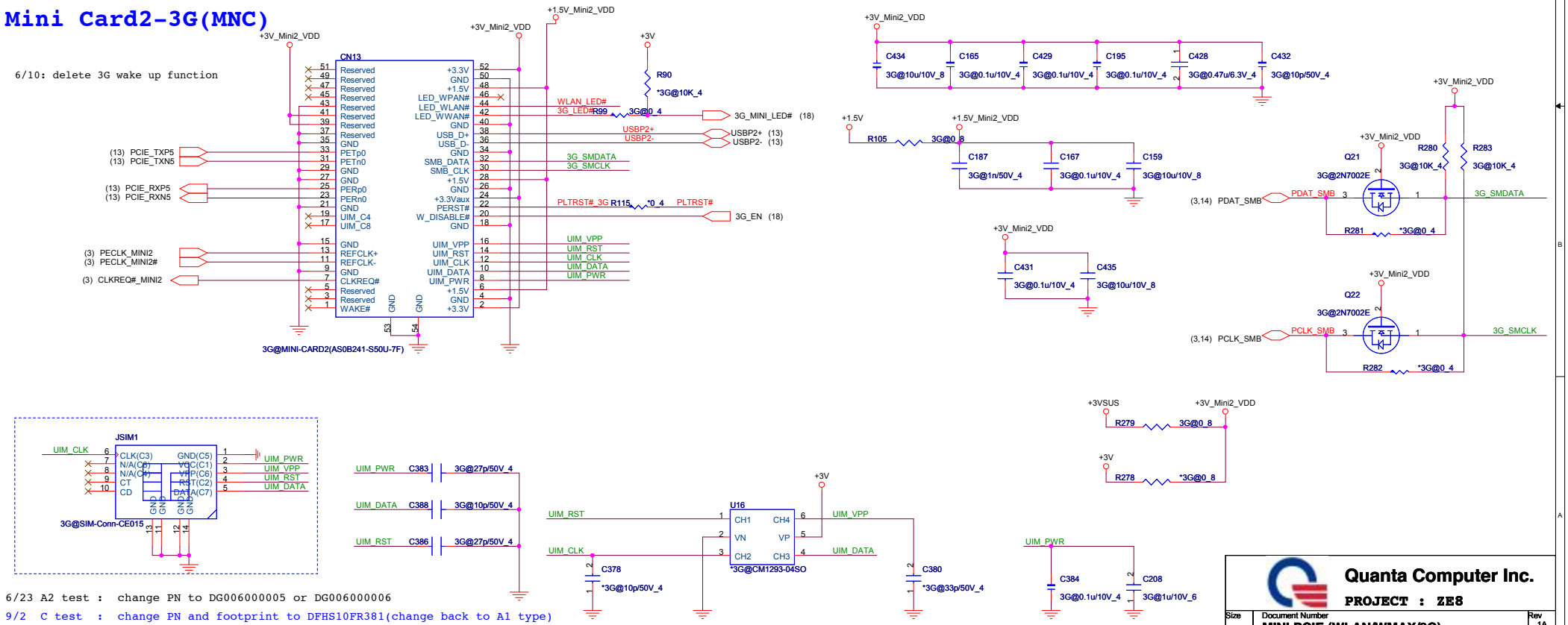
Size	Document Number	Rev
	EC WPCE775LA0DG	1A

Date: Tuesday, September 29, 2009 Sheet 18 of 32

Mini Card1-WLAN/WMAX(MNC)



Mini Card2-3G(MNC)



6/23 A2 test : change PN to DG006000005 or DG006000006

9/2 C test : change PN and footprint to DFHS10FR381(change back to A1 type)

Layout : C431 and C252 place near JSIM2

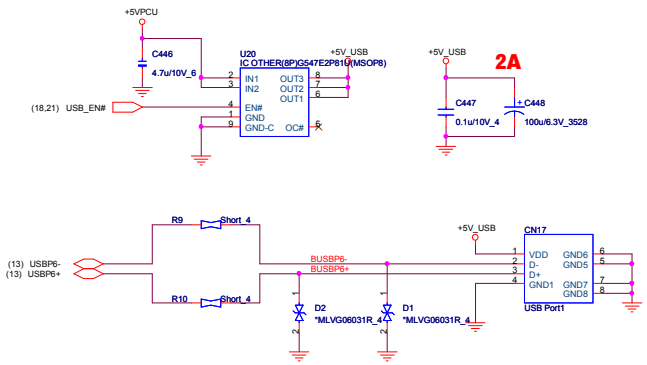
Quanta Computer Inc.

PROJECT : ZE8

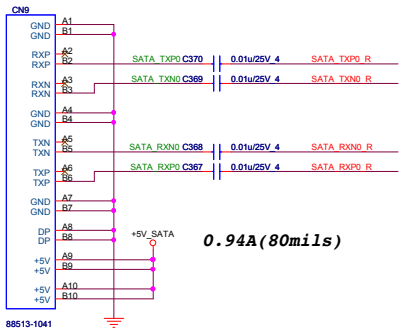
Size	Document Number	Rev
	MINI PCIE (WLAN/WMAX/3G)	1A

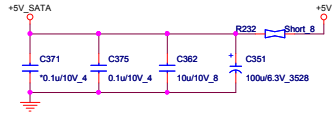
Date: Tuesday, September 29, 2009 Sheet 19 of 32

MB USB (USB)



2.5" SATA HDD(HDD)

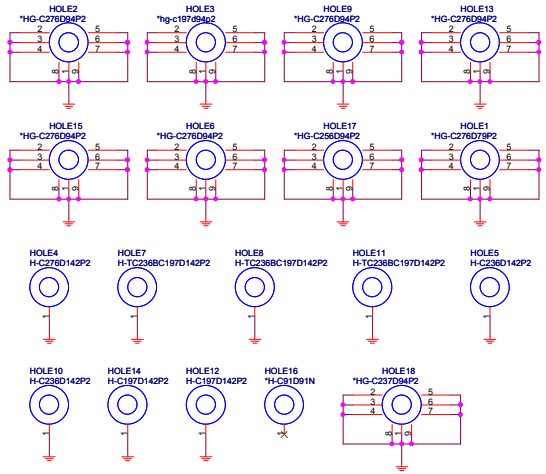




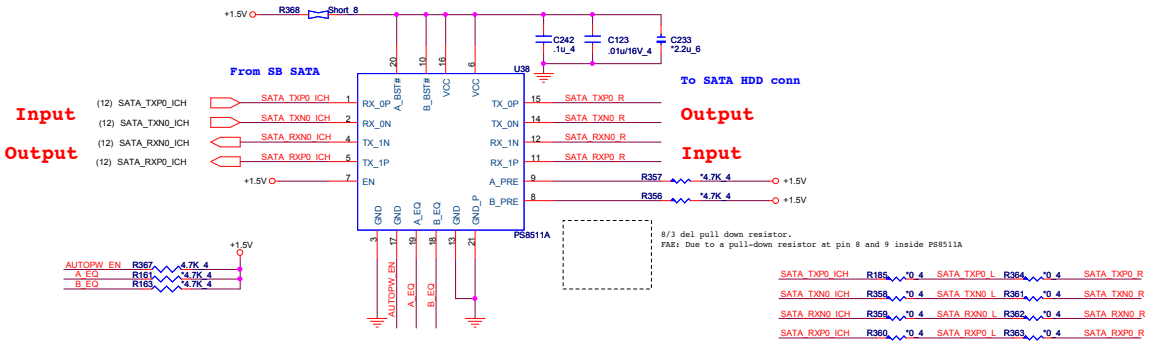
SATA ESD(EMC)

8/5 : because of the space is not enough, so, del SATA ESD U12 and C363.

HOLE (EXC)



SATA RE-DRIVER IC(XXX)



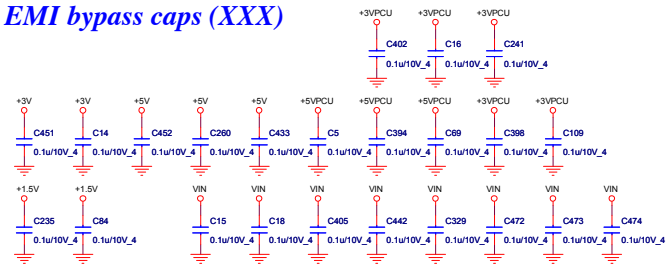
PARADE : PS8511A

PIN 18,19	Input Equalization setting: Internal pull down ~150Kohm A_EQ/B_EQ = LOW: For short and medium length PCB traces (default) A_EQ/B_EQ = HIGH: For long length PCB traces
PIN 8,9	Output Pre-emphasis Setting: Internal pull down ~150Kohm A_PRE/B_PRE = LOW, Pre-emphasis disabled (default) A_PRE/B_PRE = HIGH, Pre-emphasis enabled
PIN 10,20	Output Level Boost setting: Internal pull up~150Kohm A_BST#/B_BST# = HIGH, SATAi/m output level 400~700mVpp (default--SATA internal) A_BST#/B_BST# = LOW, SATAx output level 800~1200mVpp
PIN 17	Automatic Power Saving Enable: Internal pull down~150Kohm AUTOPW_EN = HIGH, automatic power saving enable (default) AUTOPW_EN = LOW, automatic power saving disable

PARADE : PS8511A

EN	A_PRE	B_PRE	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (3.5dB)	0dB
1	0	1	0dB	Pre-emphasis (3.5dB)
1	1	1	Pre-emphasis (3.5dB)	Pre-emphasis (3.5dB)

EMI bypass caps (XXX)



PAD

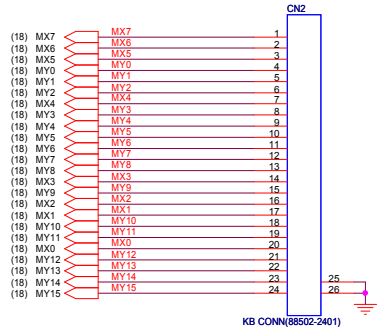
Quanta Computer Inc.

PROJECT : ZE8

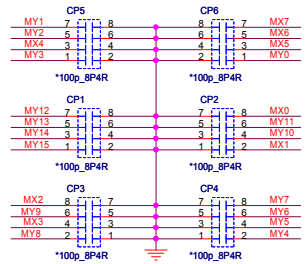
Size	Document Number	Rev
	USB/HDD/HOLE	1A

Date: Tuesday, September 29, 2009 Sheet 20 of 32

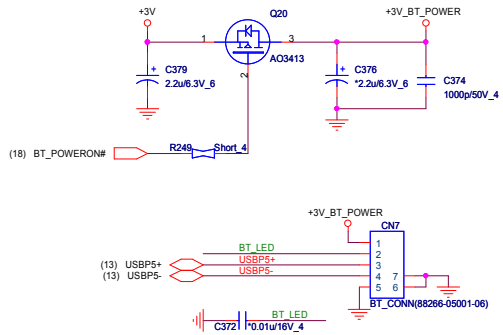
Keyboard(KBC)



For EMI Reserve Caps for debug

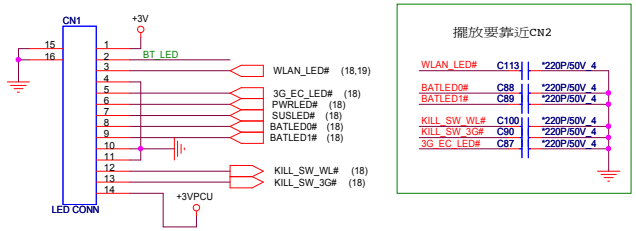


BuleTooth (BTM)

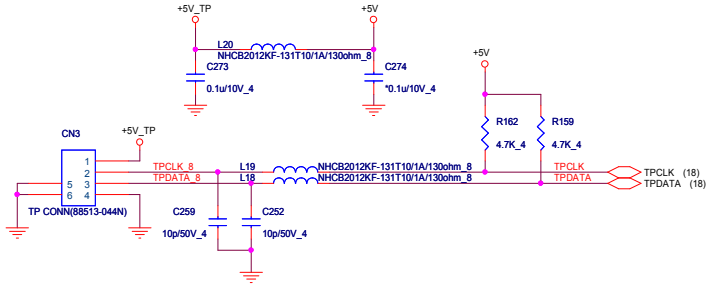


Be careful that bluetooth module PIN 2 is GND and PIN 5 is BT_LED.

LED D/B (UIF)



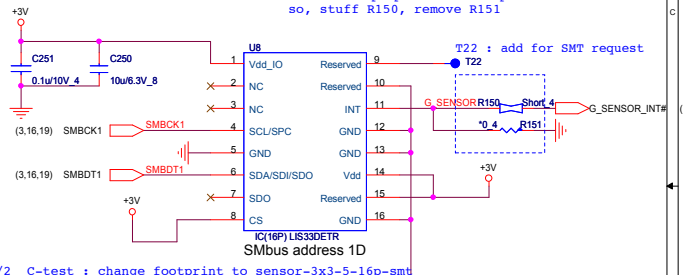
Touch Pad D/B (TPD)



G SENSOR(GSR)

A0 test : have free fall function, stuff R329, if not, stuff R327 just can stuff one of them

6/23 A2 test : per Acer request, use interrupt pin to detect panel status so, stuff R150, remove R151

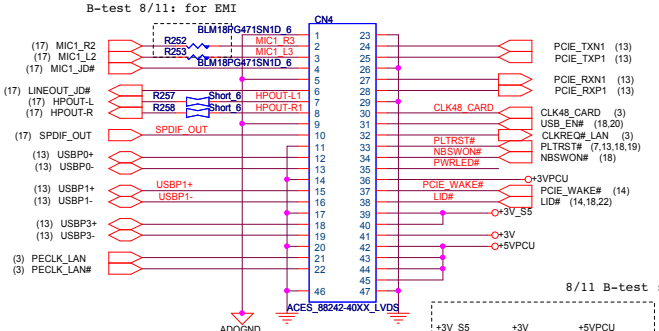


9/2 C-test : change footprint to sensor-3x3-5-16p-smt
9/24 Ramp-test : change footprint to sensor-3x3-5-16p-smt.(part two)

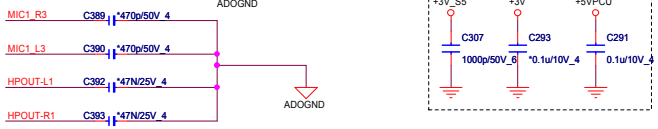
FAE : Because of internal pull-high in SDO, I2C address for SDO floated is the same as that for SDO high

Card Reader/USB DB CONNECTER(MMC)/Power Connector

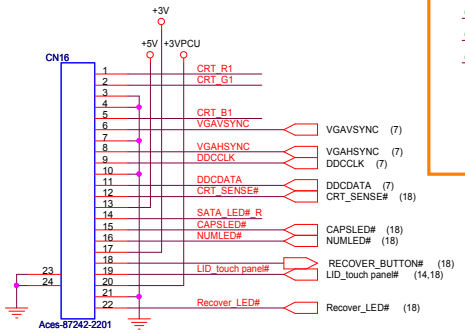
B-test 8/11: for EMI

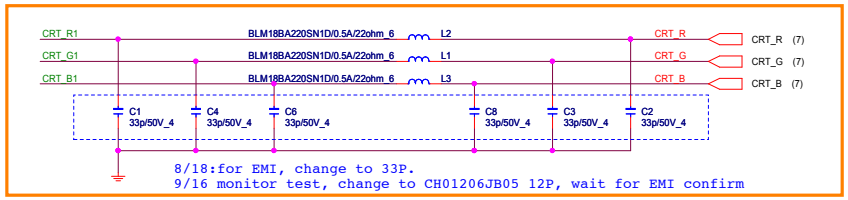


8/11 B-test : for EMI



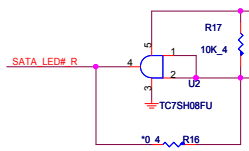
CRT D/B (CRT)

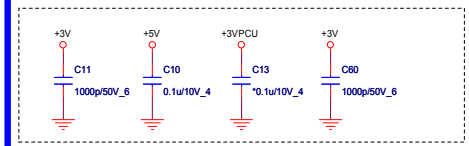




8/18:for EMI, change to 33P.
9/16 monitor test, change to CH01206JB05 12P, wait for EMI confirm

For EMI





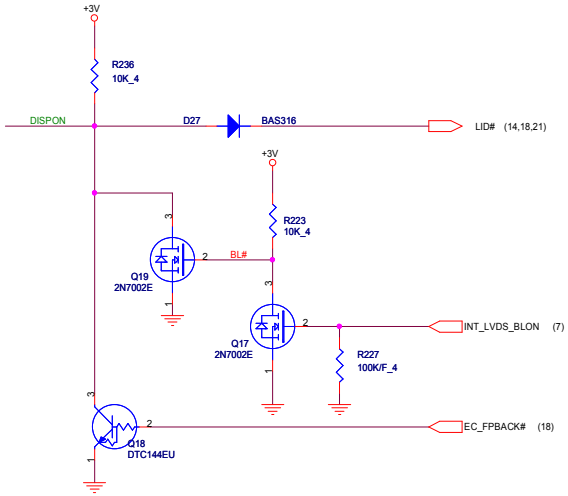
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	KB/BT/PR/TP/LAN/LED/CR Connects	1A

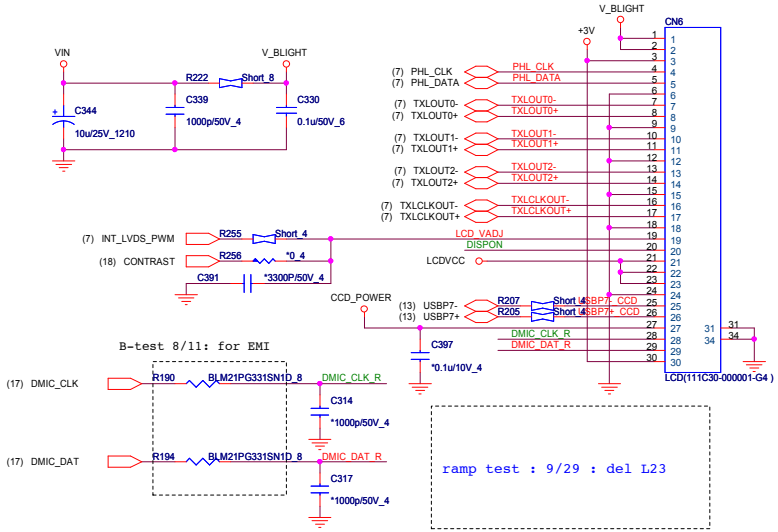
Date: Tuesday, September 29, 2009 Sheet 21 of 32

Backlight Control(LDS)

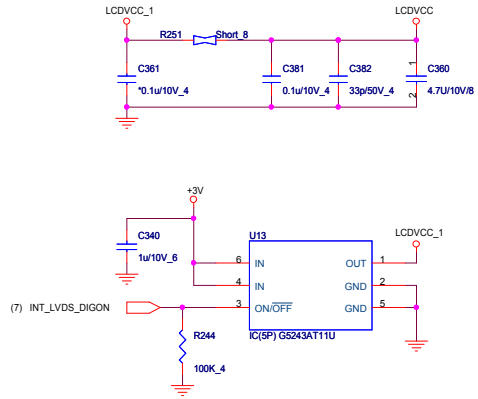


LED Panel(LDS)

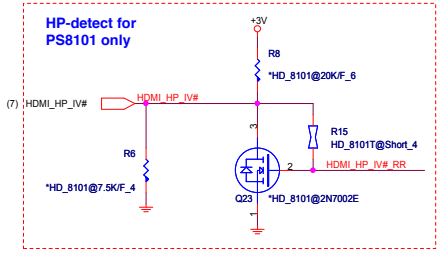
C test: 8/31: exchange V_BLIGHT and LCDVCC pin define



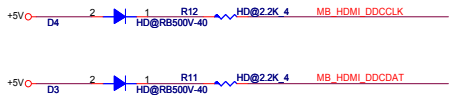
LED Panel POWER SWITCH(LDS)



HDMI(HDM)

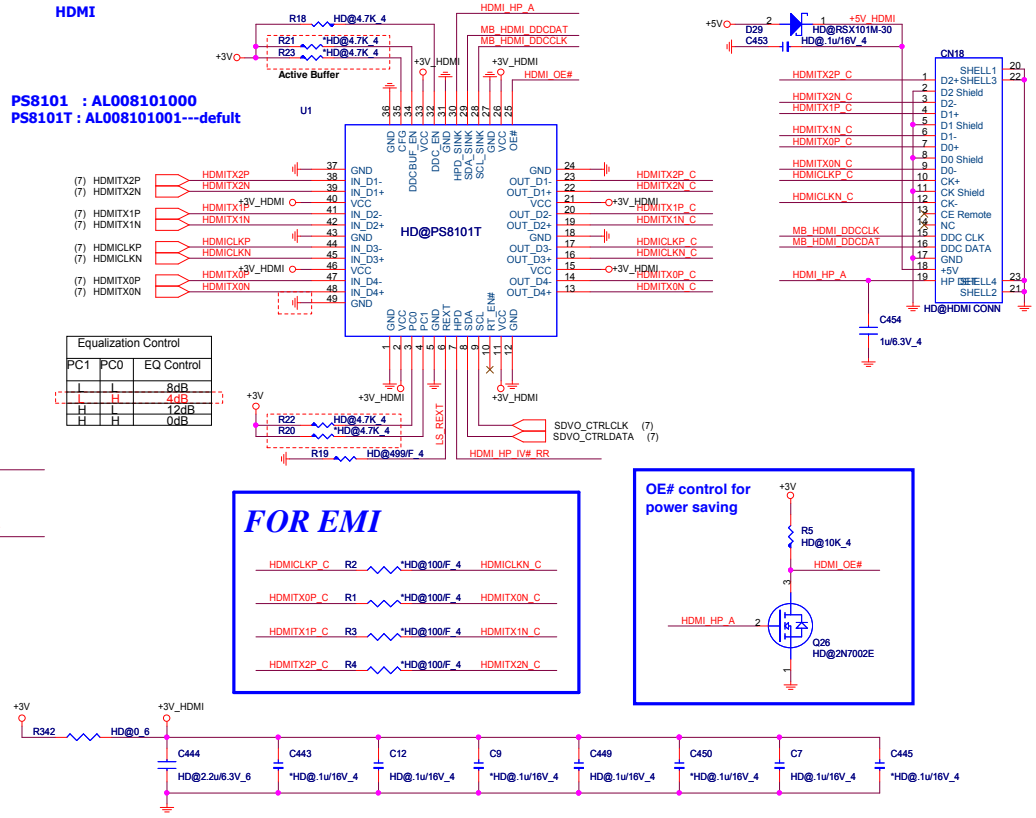


SDVO I2C Control



	PS8101 AL008101000	PS8101T AL008101001
pin 7	HPD	HPD#
pin 34	DDCBUF_EN	CFG0
pin 35	CFG	CFG1

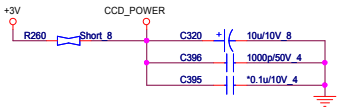
HDMI



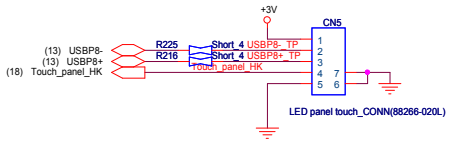
FOR EMI

OE# control for power saving

Camera(CCD)



LED touch Panel connector (LDS)



ramp test : 9/29 : del L24

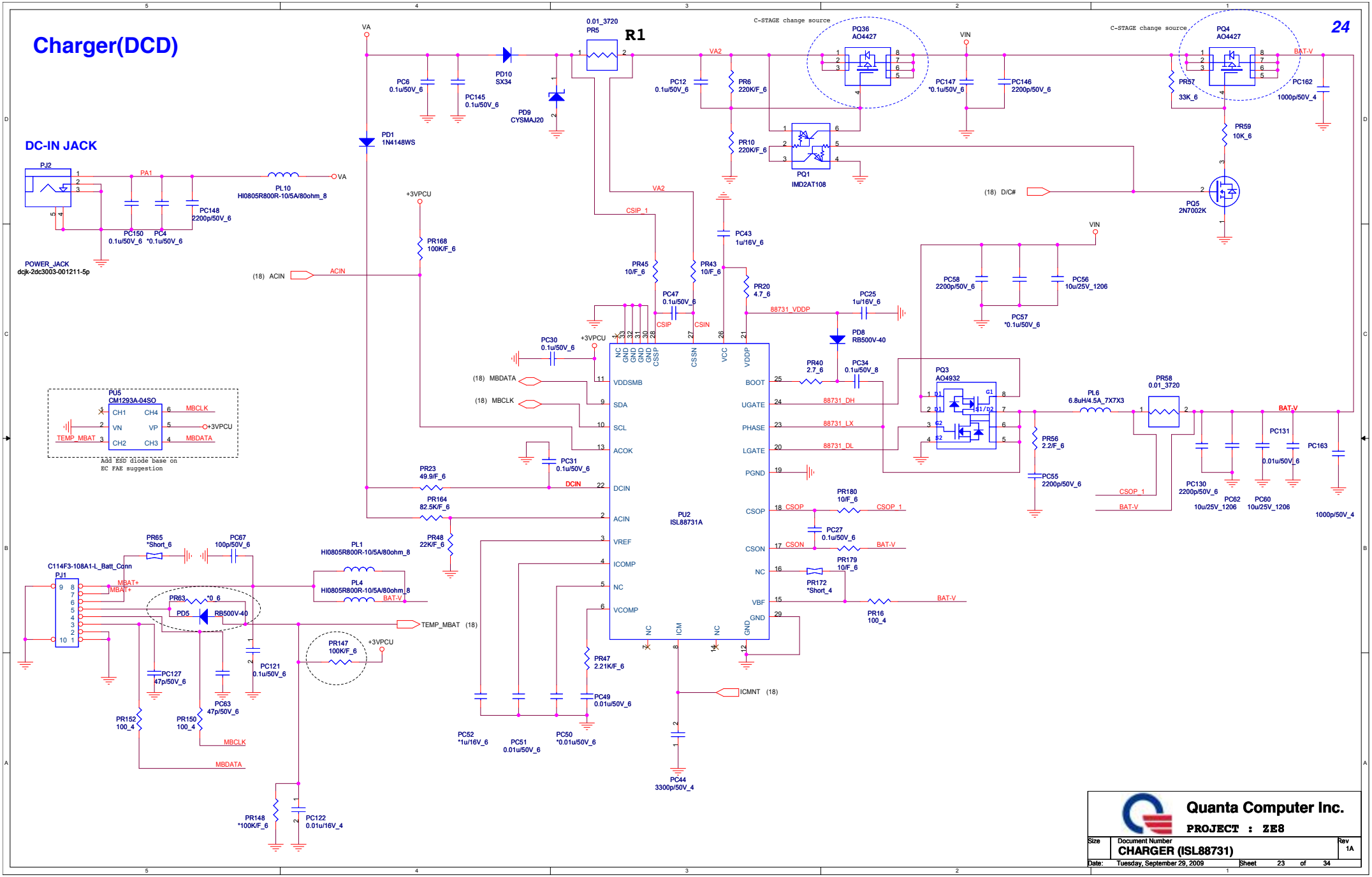
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	LED Panel/CCD/HDMI	1A

Date: Tuesday, September 29, 2009 Sheet 22 of 32

Charger(DCD)

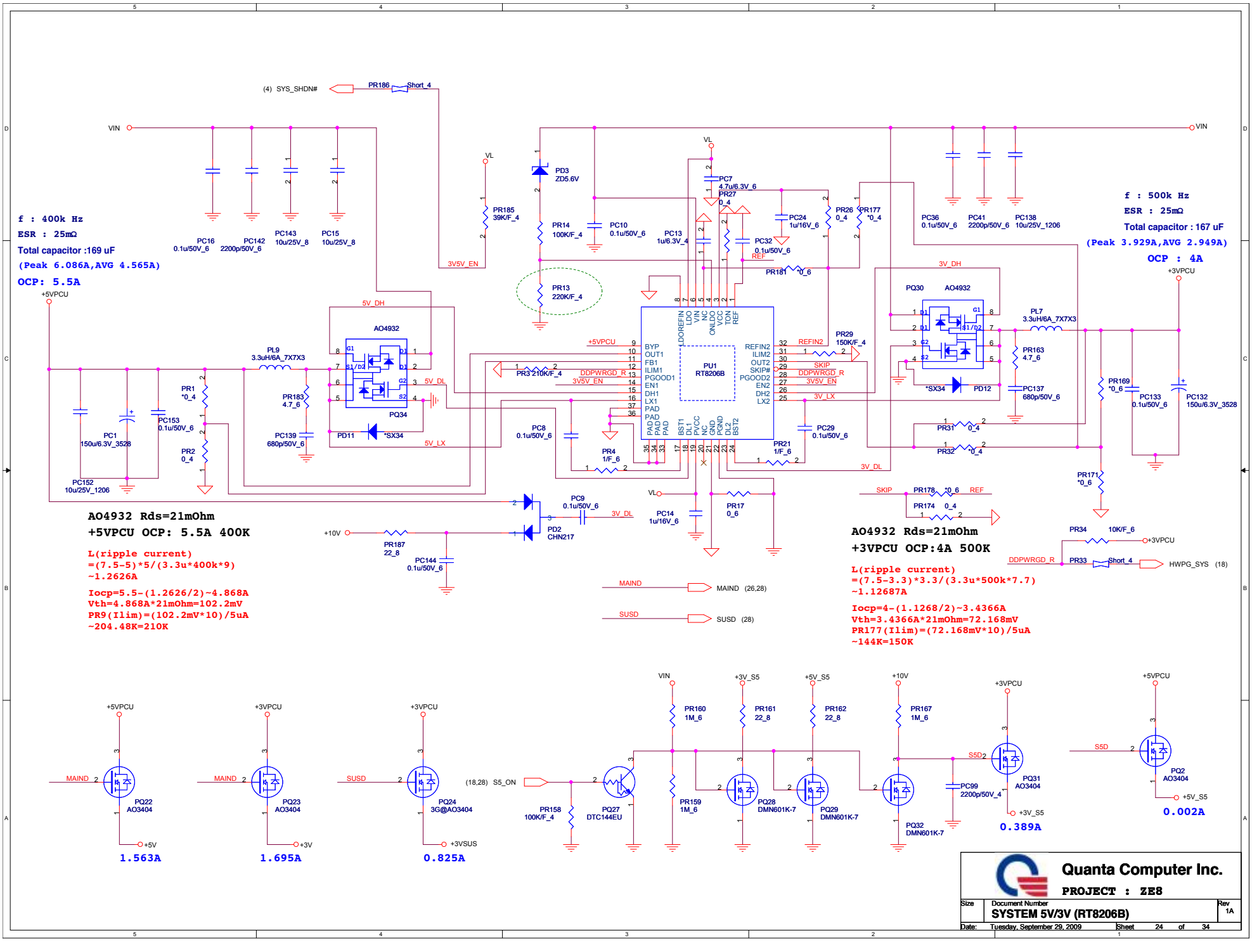


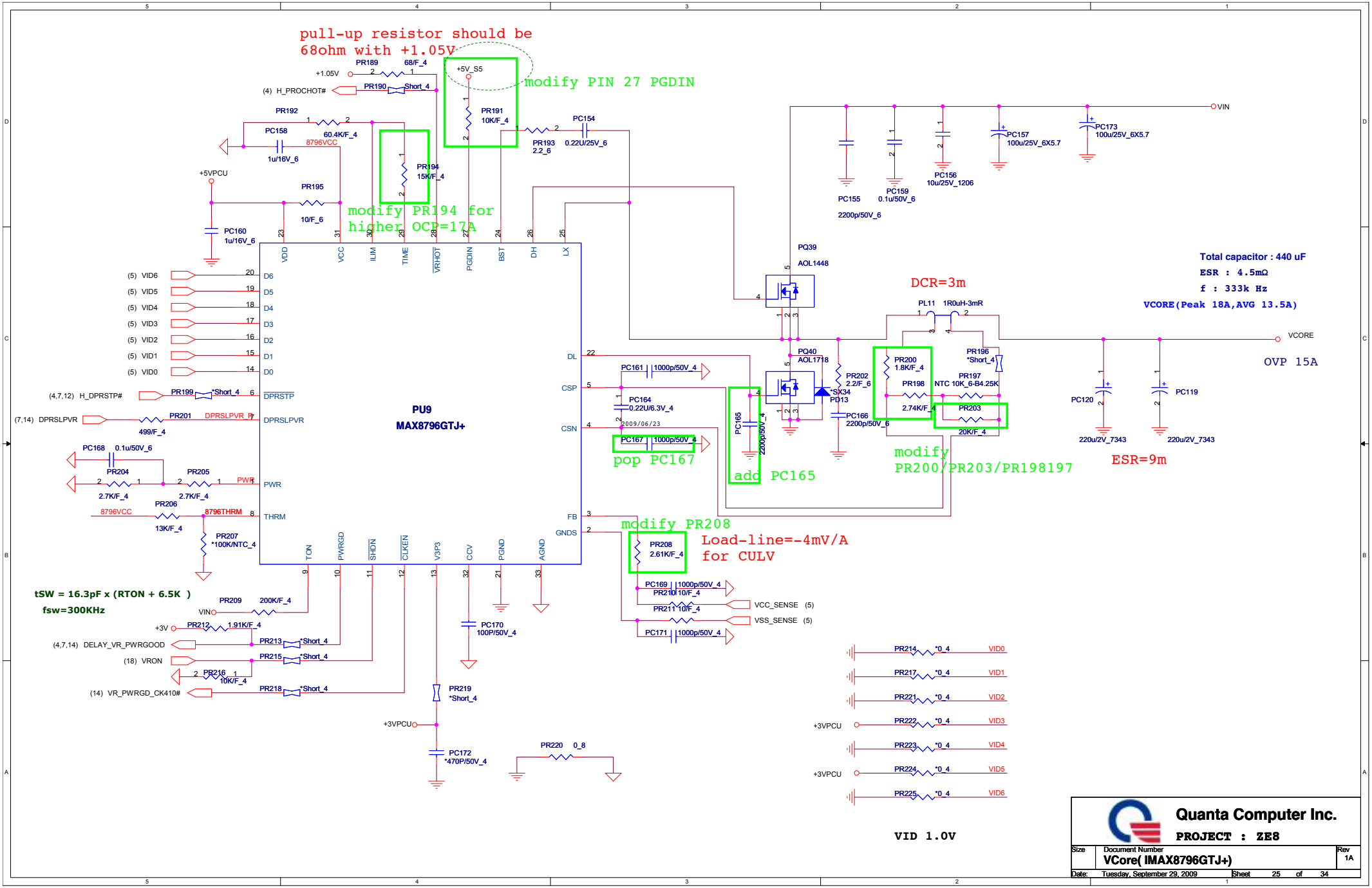
Quanta Computer Inc.

PROJECT : ZE8

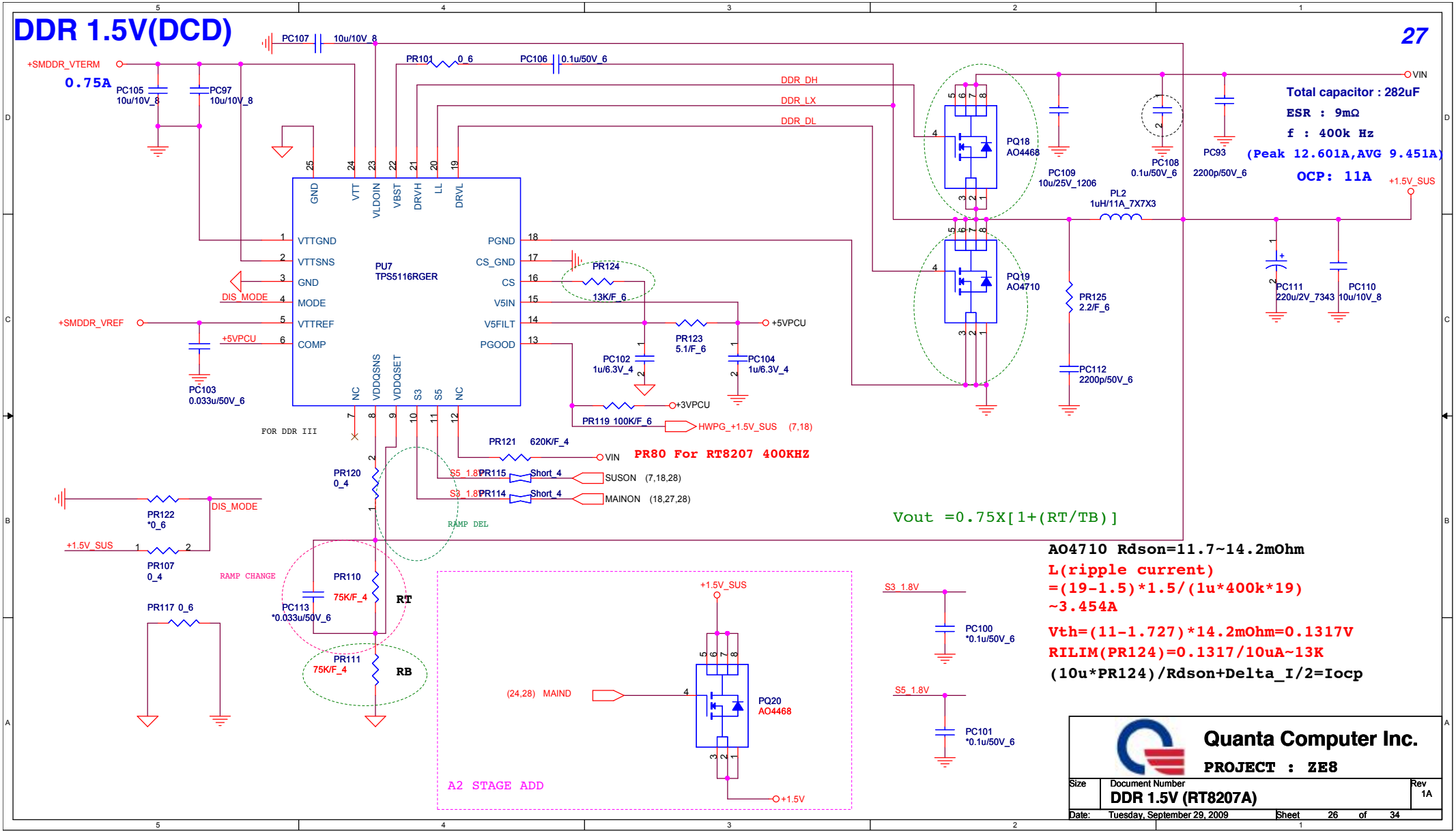
Size	Document Number	Rev
	CHARGER (ISL88731)	1A

Date: Tuesday, September 29, 2009 Sheet 23 of 34


f : 400k Hz
ESR : 25mΩ
Total capacitor :169 uF
(Peak 6.086A,AVG 4.565A)
OCP: 5.5A
f : 500k Hz
ESR : 25mΩ
Total capacitor : 167 uF
(Peak 3.929A,AVG 2.949A)
OCP : 4A
AO4932 Rds=21mOhm
+5VPCU OCP: 5.5A 400K
L(ripple current)
=(7.5-5)*5/(3.3u*400k*9)
~1.2626A
Iocp=5.5-(1.2626/2)~4.868A
Vth=4.868A*21mOhm=102.2mV
PR9(Ilim)=(102.2mV*10)/5uA
~204.48K=210K
AO4932 Rds=21mOhm
+3VPCU OCP:4A 500K
L(ripple current)
=(7.5-3.3)*3.3/(3.3u*500k*7.7)
~1.12687A
Iocp=4-(1.1268/2)~3.4366A
Vth=3.4366A*21mOhm=72.168mV
PR177(Ilim)=(72.168mV*10)/5uA
~144K=150K
PU1
RT8206B
PQ22
AO3404
1.563A
PQ23
AO3404
1.695A
PQ24
3G@AO3404
0.825A
PQ27
DTC144EU
PQ28
DMN601K-7
PQ29
DMN601K-7
PQ32
DMN601K-7
PQ31
AO3404
0.389A
PQ2
AO3404
0.002A
Quanta Computer Inc.
PROJECT : ZE8
Size
Document Number
SYSTEM 5V/3V (RT8206B)
Rev
1A
Date: Tuesday, September 29, 2009
Sheet 24 of 34


pull-up resistor should be 68ohm with +1.05V
modify PIN 27 PGDIN
modify PR194 for higher OCP=17A
PU9
MAX8796GTJ+
DCR=3m
Total capacitor : 440 uF
ESR : 4.5mΩ
f : 333k Hz
VCORE(Peak 18A,AVG 13.5A)
OVP 15A
ESR=9m
pop PC167
add PC165
modify PR200/PR203/PR198197
modify PR208
Load-line=-4mV/A for CULV
tSW = 16.3pF x (RTON + 6.5K)
fsw=300KHz
VID 1.0V
Quanta Computer Inc.
PROJECT : ZE8
Document Number
VCore(IMAX8796GTJ+)
Rev 1A
Date: Tuesday, September 29, 2009
Sheet 25 of 34

DDR 1.5V(DCD)



AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A

Vth=(11-1.727)*14.2mOhm=0.1317V

RILIM(PR124)=0.1317/10uA~13K

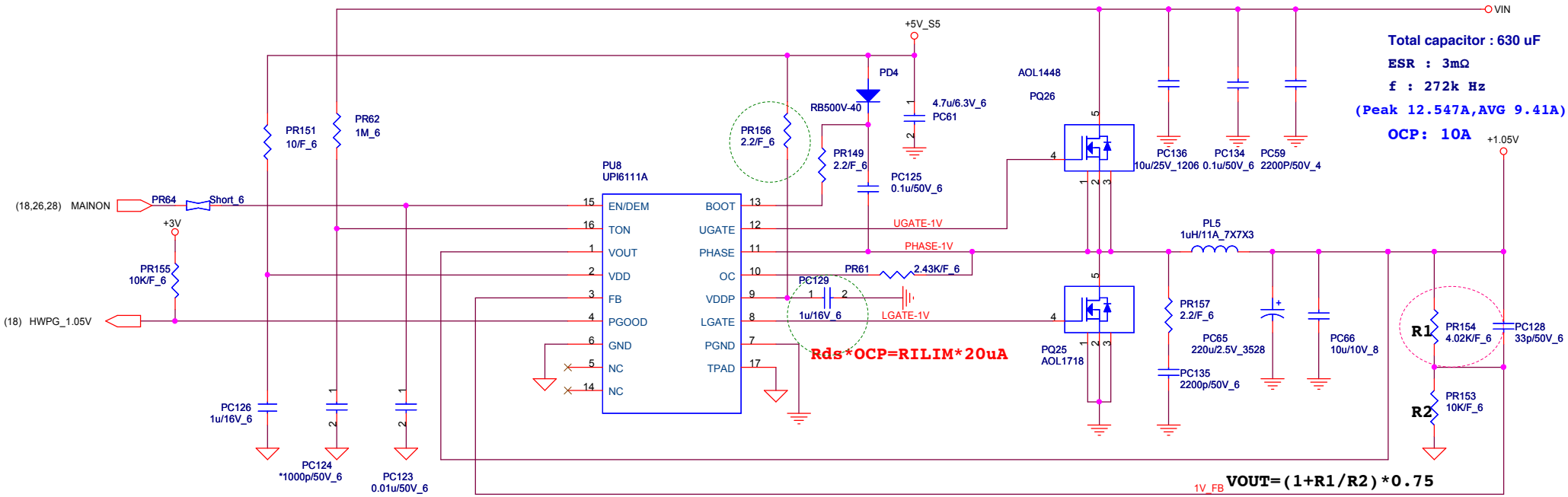
(10u*PR124)/Rdson+Delta_I/2=Iocp

Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	DDR 1.5V (RT8207A)	1A

Date: Tuesday, September 29, 2009 Sheet 26 of 34



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1718 Rdson=4.6mOhm

OCP=10-0.8A

L(ripple current)

=(19-1.05)*1.05/(1u*272k*19)

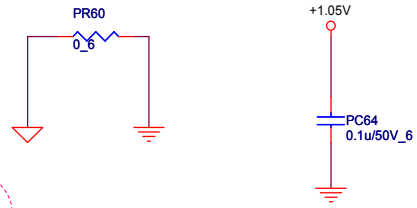
~3.646A

4.6m*10=RILIM*20uA

RILIM(PR61)=2.3K--- 2.43K

RAMP CHANGE

	743 CPU	Other CPU
PR154	4.22K (CS24223F917)	4.02K (CS24023F928)



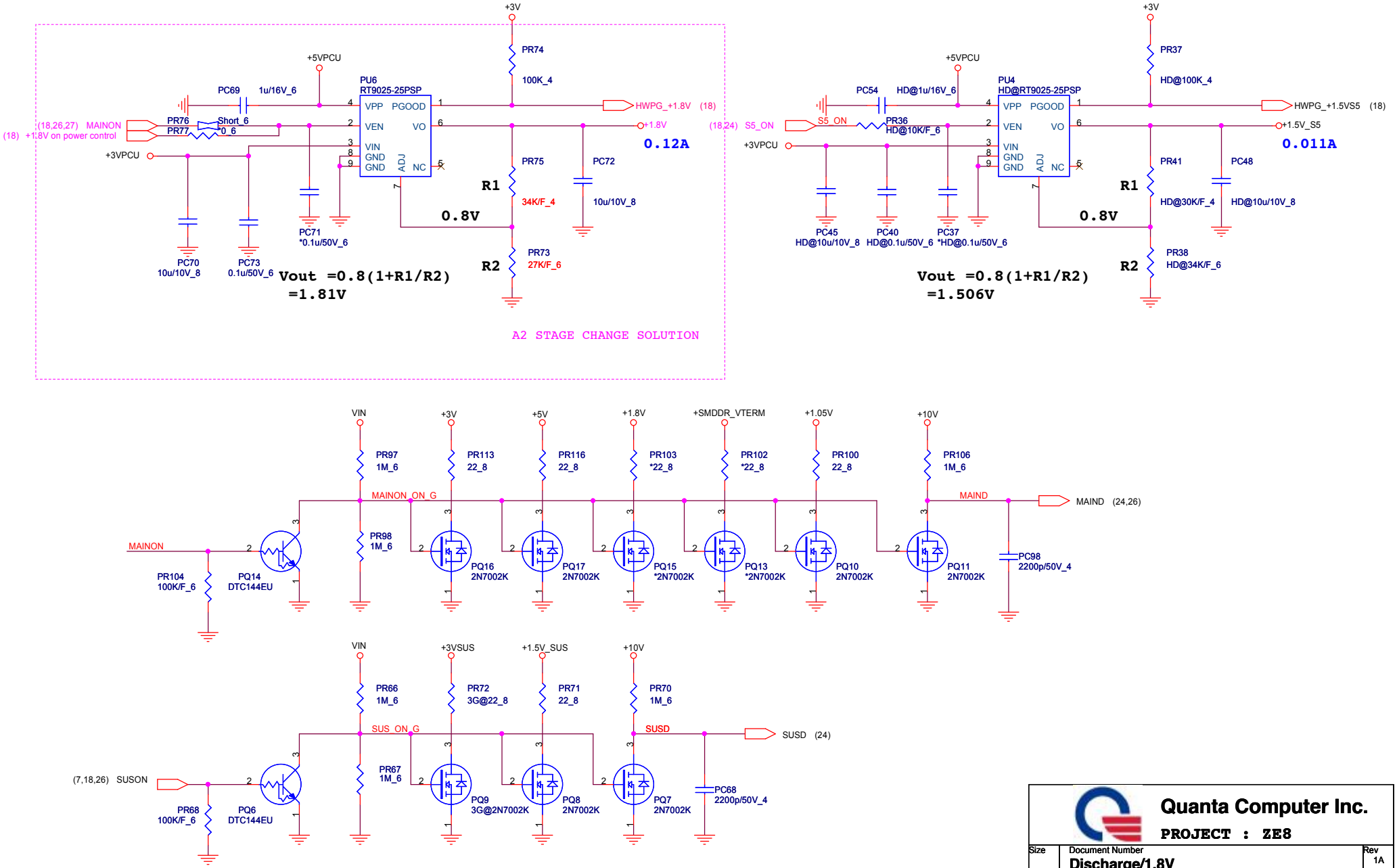
Quanta Computer Inc.

PROJECT : ZE8

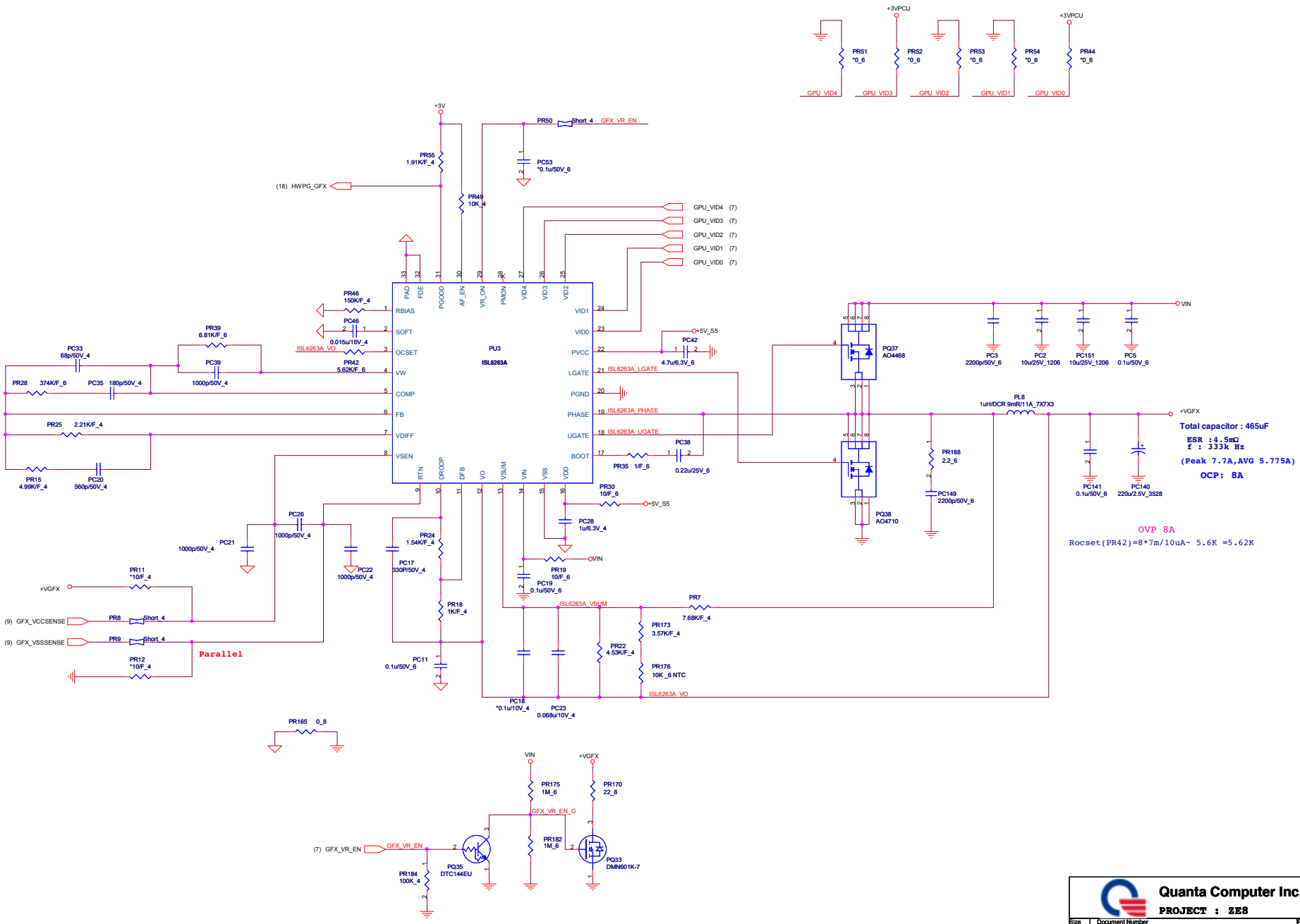
Size	Document Number	Rev
	VCCP 1.05V (RT8202A)	1A

Date: Tuesday, September 29, 2009 Sheet 27 of 34

Discharger/1.8V(DCD)



Quanta Computer Inc.		
PROJECT : ZE8		
Size	Document Number: Discharge/1.8V	Rev 1A
Date: Tuesday, September 29, 2009	Sheet 28 of 34	

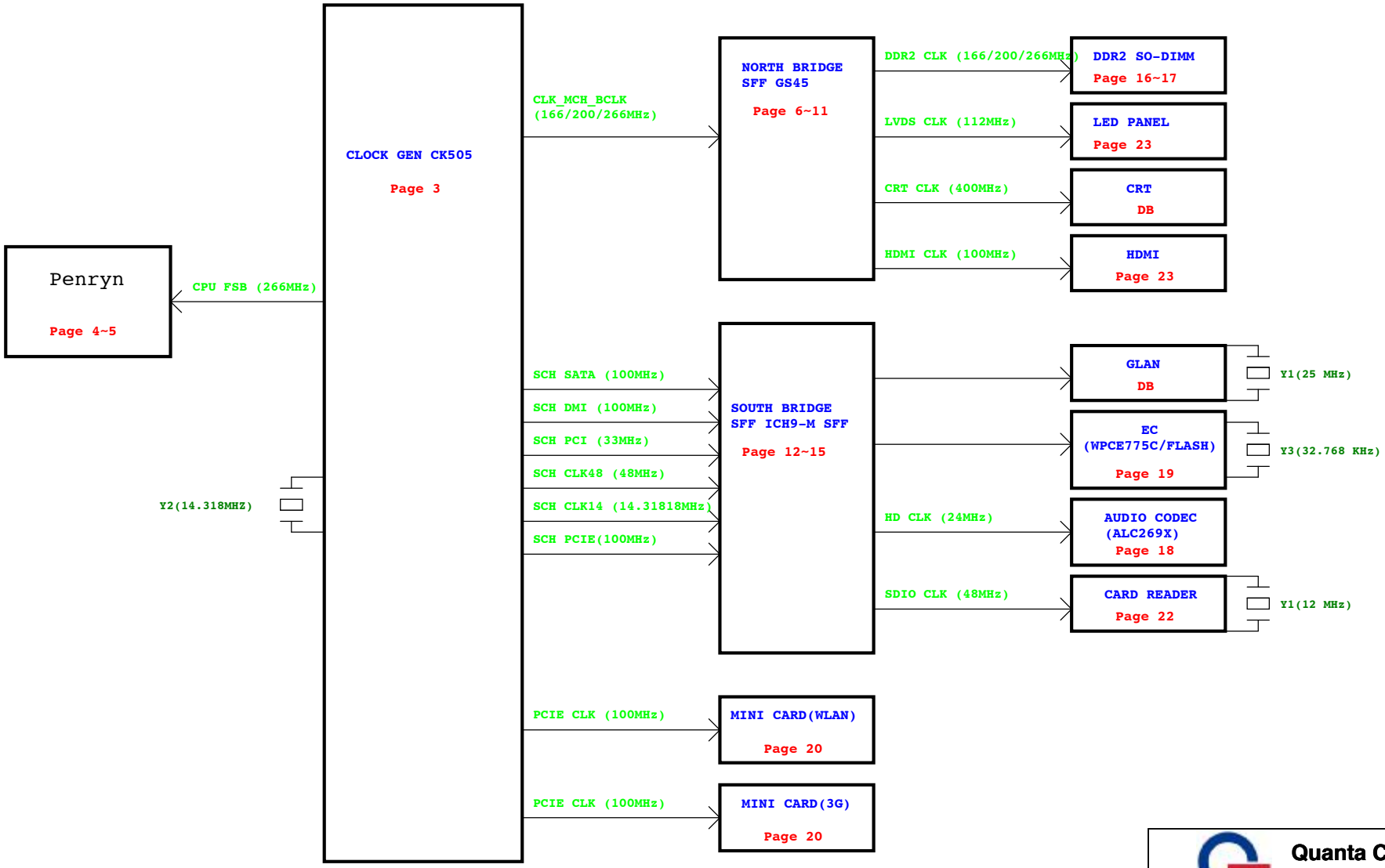


Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	1.05V_GFX	1A

Date: Tuesday, September 29, 2009 Sheet 29 of 34



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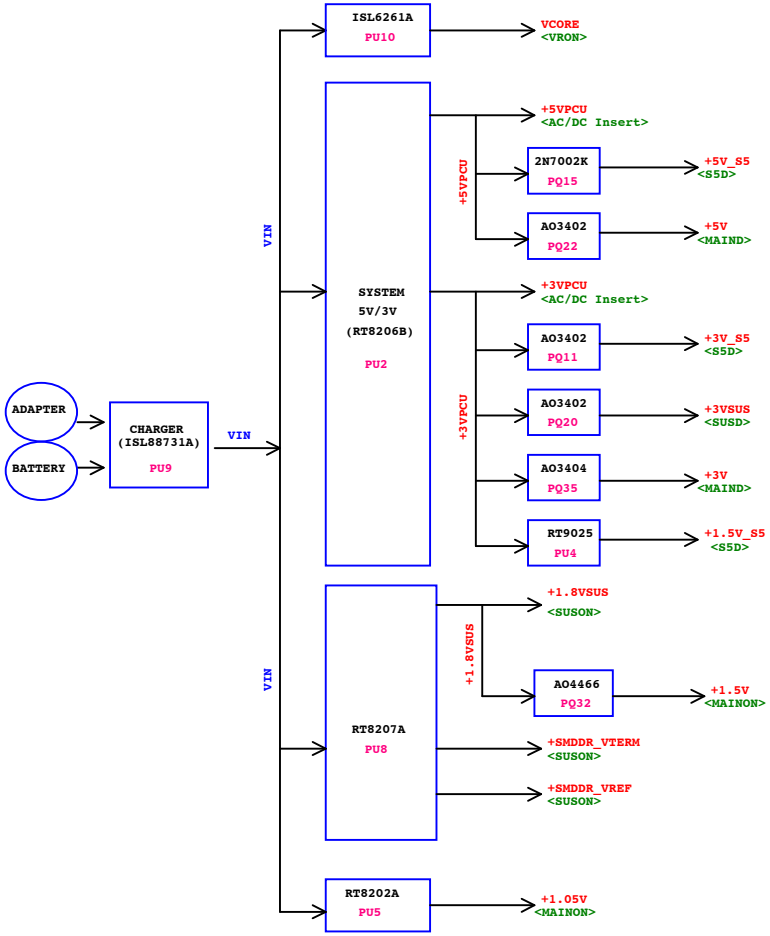
PROJECT : ZE8

Size	Document Number	Rev
	Clock Distribution Diagram	1A

Date: Tuesday, September 29, 2009 Sheet 30 of 34



POWER	Distribution
VCORE	CPU
+5VPCU	RTC, USB Connecter
+5V_S5	ICH9M Power
+5V	ICH9M Power, CRT, Audio Codec, SATA HDD, Touch Pad ,HDMI
+3VPCU	RTC, LED Power, CRT, EC, ID , SPI Flash , Green Adapter
+3V_S5	ICH9M Power, CR
+3VSUS	3G
+3V	CLK_GEN Power, Thermal Sensor Power, NB Power, SB, DDRII Power, Audio Codec, LCD Power, WLAN/WMAX, 3G, Card Reader, BT, EC, LED, CRT, CAMERA
+1.5V_S5	ICH9M Power
+1.8VSUS	NB Power, DDRII SO-DIMM
+1.5V	CPU, NB, SB, AUDIO Codec, WLAN/WMAX, 3G
+SMDDR_VTERM	DDRII SO-DIMM
+SMDDR_VREF	DDRII SO-DIMM
+1.05V	CLK_GEN, CPU, NB, SB

CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	Differential CPU clock
CPU_0#	60	CLK_CPU_BCLK#	
CPU_1	58	CLK_MCH_BCLK	Differential NB GS45 clock
CPU_1#	57	CLK_MCH_BCLK#	

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	96MHz DOT clock for NB GS45
SRC0#/DOT96#	21	DREFCLK#	
LCDCLK/27M	24	DREFSSCLK	Clock output for NB GS45 graphic contoller
LCDCLK#/27M_SS	25	DREFSSCLK#	
SRC2	28	PECLK_SATA	Differential Serial Reference Clock for SB ICH9M SATA
SRC2#	29	PECLK_SATA#	
SRC3/CR#_C	31	PECLK_ICH	Differential Serial Reference Clock for SB ICH9M
SRC3#/CR#_D	32	PECLK_ICH#	
SRC4	34	PECLK_LAN	Differential Serial Reference Clock for on board LAN
SRC4#	35	PECLK_LAN#	
SRC6	48	PECLK_MINI2	Differential Serial Reference Clock for Mini Card 2
SRC6#	47	PECLK_MINI2#	
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		No use
SRC8#/CPU_ITP#	53		
SRC9	37	PECLK_MINI1	Differential Serial Reference Clock for MINI CARD 1
SRC9#	38	PECLK_MINI1#	
SRC10	41	PECLK_3GPLL	Differential Serial Reference Clock for NB GS45
SRC10#	42	PECLK_3GPLL#	
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

Model	REV	DATE	CHANGE LIST	NOTE
ZE8	A1A		PAGE23 :move LED touch Panel hall sensor to LAN DB	ECN Release
			PAGE20 : reserve R179 , R183 for 3G wake up function	
			PAGE5 : Del C128,C173,C149,C171,C130,C131,C133,C169,C181,C177,C132,C175,C140,C138,C185,C154,C135,C92,C184,C106,C117,C156,C186,C153	
			for placeing C386 in CPU BGA TOP side	
			PAGE18 :change U14 footprint to qfn48-7x7-5-58p-0_9h	
			PAGE23 :change CN18 PN to DFHD19MR053	
			PAGE23 :Add L28 and L29 for CCD and Touch screen USB signals	
			PAGE23 :change CN18 footprint to hdmi-100042mr019m21hzr-19p-v	
			PAGE23 :change CN19 footprint to 85204-0500x-5p-l	
			PAGE23 :add 5V power trace to CN19 for touch screen IC	
			PAGE19 :FAE suggest that add R352 for VCC latch up	
			PAGE19 : FAE suggest that change C347 and C350 value from 15p to 6.8p	
			PAGE10 : add stitching caps C149,C153 and C154 for DMI signals	
			PAGE14 : add stitching caps C156,C169 and C171 for DMI signals	
			PAGE20 : add C431 for SIM Card to filter power noise.	
			PAGE20 : change U10 PN from AL001293003 to AL001293000	
			PAGE21 : reserve ESD protection U11 for SATA signals.	
			PAGE23 : del +5V signal of CN19	
			PAGE18 : add stitching caps C432,C438 for Audio signals	
			PAGE21 : del hole 19	
			PAGE22 : reserve C439, C440,C445,C446,C447,C448 for EMI	
			PAGE23 : reserve C106 for EMI	
			PAGE 19, 20 : del R179, R183 and 3G wake up signals of 3G wake up function	
			PAGE19 : add D30 for WLAN_LED# connect from WALN connector to EC	
			PAGE19 : add 3G_EC_LED# signal from EC to LED connector CN2	
			PAGE19 : change R233 to D31 for leakage issue.	
			PAGE22 : del C426 due to don't need 3G_MINI_LED# singal from 3G connector to LED connector CN2	
			PAGE21 : add EMI bypass caps	
			PAGE23 : HDMICLKP swap to HDMITX0P,HDMICLKN swap to HDMITX0N,HDMICLKP_C swap to HDMITX0P_C,HDMICLKN_C swap to HDMITX0N_C	
			6/13 : PAGE10 : change C63 and C208 value from 220u to 10u.	
			6/15 : PAGE18 : due to layout, add 9 GND pin for U14	
			6/15 : PAGE19 and 23 : add Touch_panel_HK signal for hot key on touch panel	
			6/16 : PAGE 23 : change R14 to C454 of CN18 for HDMI detect issue	
			6/18 : PAGE 23 : change CN5 PN to DFHD05MRD98	
			6/18 : PAGE 19 : change U14 PN to AKE38ZA0Q00	
	B1A			
			6/22 : PAGE 21 : change CN17_PN to DFHS04FR269	
			6/22 : PAGE 24 : change PJ1_PN to DFHD08MR085	
			6/23 : PAGE 22 : Per Acer request, use interrupt pin of G-sensor to detect panel status ,so , stuff R150, remove R151	
			6/25 : PAGE 19 : EC add +1.5V on power control net name to control 1.5V	
			6/25 : PAGE 22 : connect G-sensor interrupt signal to SB PIRQE#	
			6/26 : PAGE 26 : change V-core solution to Maxim IC	
			6/26 : PAGE 24 : add PD20 in TEMP_MBAT signal	
			6/29 : PAGE 9 : change C212 from 330U to 10U for placement issue	
			6/30 : PAGE 16 : change DDR2 to DDR3	
			7/2 : PAGE 14 : LID_touch panel# change from GPIO19 to GPIO7 (SCI)	
			7/2 : PAGE 16 : change DDR3 connector footprint to H=5.2mm	
			7/6 : PAGE 18,21 : add RECOVER_BUTTON# signal in EC and CRT DB	
			7/7 : PAGE 18,21 : add RECOVER_LED# signal in EC and CRT DB	
			7/7 : PAGE 24 : add PD11 and PD12	
			7/7 : PAGE 25 : add PD13	
			7/7 : PAGE 20 : add nut on Hole 7, Hole 8 and Hole 11	
			7/7 : PAGE 18 : add R355 for power consumption issue,Vendor suggest to place it close to EC.	
			7/8 : PAGE 18 : add D30 for current leakage issue of 3G_EC_LED# signal.	
			7/9 : PAGE 18 : add D31 to prevent current leakage of Recover_LED# signal.	
			7/10 : PAGE 19 : change the direction of Q21 and Q22 to prevent the current leakage	
			7/10 : PAGE 3 : follow vendor suggestion to change C226 from 33p to 27p.	
			7/13 : PAGE 18 : follow vendor suggestion to change C337 and C343 from 6.8p to 15p.	

Model	REV	DATE	CHANGE LIST	NOTE
ZE8	C1A		7/23 : PAGE 20 : change CN17 footprint to usb-04wl4b-4p-r-v	ECN Release
			7/23 : PAGE 20 : add U38 re-driver IC for SATA connector	
			7/29 : PAGE 19 : change JSIM1 pin define to solve SIM card not detect issue	
			7/31 : PAGE 20 : add parade solution of SATA re-driver IC	
			8/4 : PAGE 20 : change footprint of U38 to qfn20-4x4-5-21p-ps8511b	
			8/6 : because of DMI reference to GND, so, del C60 C67 C61 C150 C166 C153 CAPS	
			8/6 : PAGE 20 : change Hole 18 footprint HG-C237D94P2, Hole 16 to H-C91D91N	
			8/10 : PAGE 19 : change JSIM1 PN to DFHS06FS017 and change footprint to simcard-sim-06lj3g-10p	
			8/11 : add C244 C245=220pF, add C243 =680pF,change C11= 1000pF,add C60=1000pF,change C307= 1000pF,add C363=0.1uF,change C10= 0.1uF,	
			R113 change to BLM18BA750SN1 ferrite bead,R252, R253 = ferrite bead (BLM18PG471SN1),R190, R194 = BLM21PG331SN1 for EMI	
			8/12 : change JSIM1 back to A2-test P/N and footprint.	
			8/13 : add C246,C247=220pF, add C471=0.1uF for EMI	
			8/28 : page13 : add pull high resister R160 in GNT3# pin for no video issue.	
			8/31 : page 22 : exchange V_BLIGHT and LCDVCC pin define	
			9/2 : page 19 : change PN and footprint of JSIM1 back to A1 type.	
			9/2 : page 21 : change G-Sensor footprint to sensor-3x3-5-16p-smt for SMT solder issue.	
			9/8 : page 23 : change battery connector footprint to bat-btj-08fg0b-8p-l-v for SMT issue.	
			9/8 : change R141,R303,R199,R259,R254,R174,R201,R172,R173,R217,R261,R168,R175,R249,R150,R15 to short pad	
	C3A		9/28 : change PU2 footprint from QFN28-5X5-5-33P to qfn28-5x5-5-33p-nb4	

Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Change List01	1A

Date: Tuesday, September 29, 2009 Sheet 34 of 34